Model Discovery for Analog/Mixed-Signal Circuits

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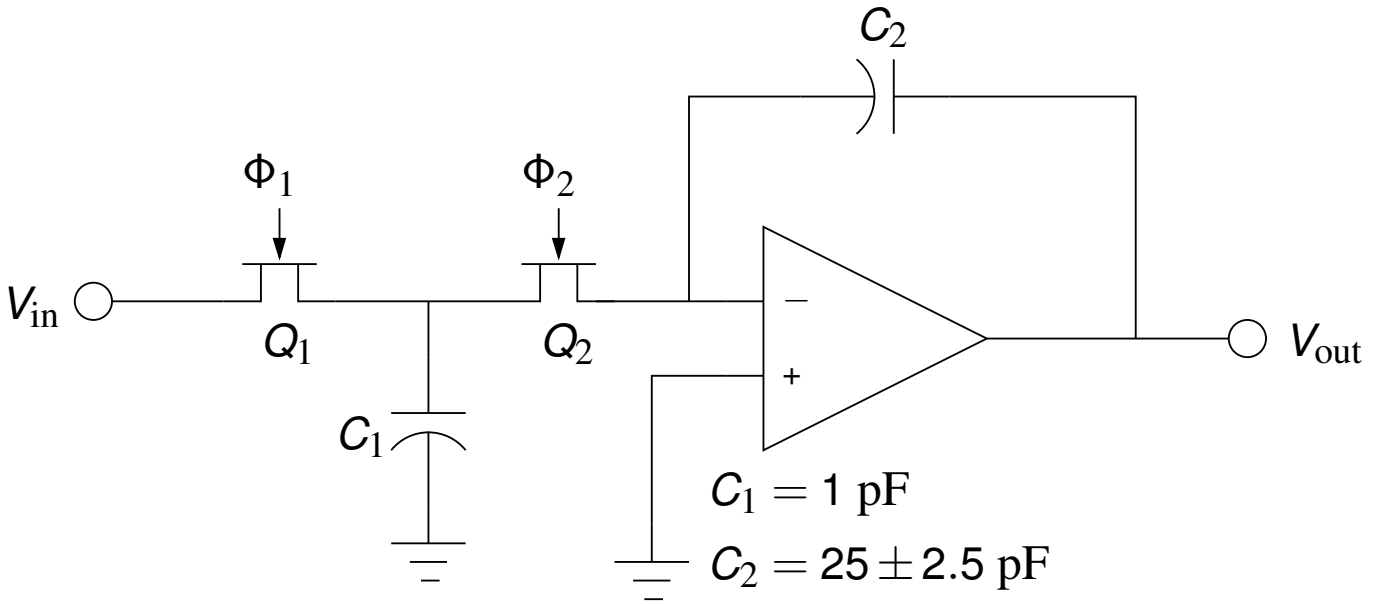
Formal Verification of Analog/Mixed-Signal Circuits

- Formal verification is a promising mechanism to validate designs in the face of noise and uncertain parameters and initial conditions.
- AMS verification is complicated by the need to construct abstract, accurate formal models of the AMS circuits.
- Verification must work with existing SPICE/SVA-based design flows.
- This talk describes a new methodology for creating these formal models for verification from SPICE-level simulation traces.

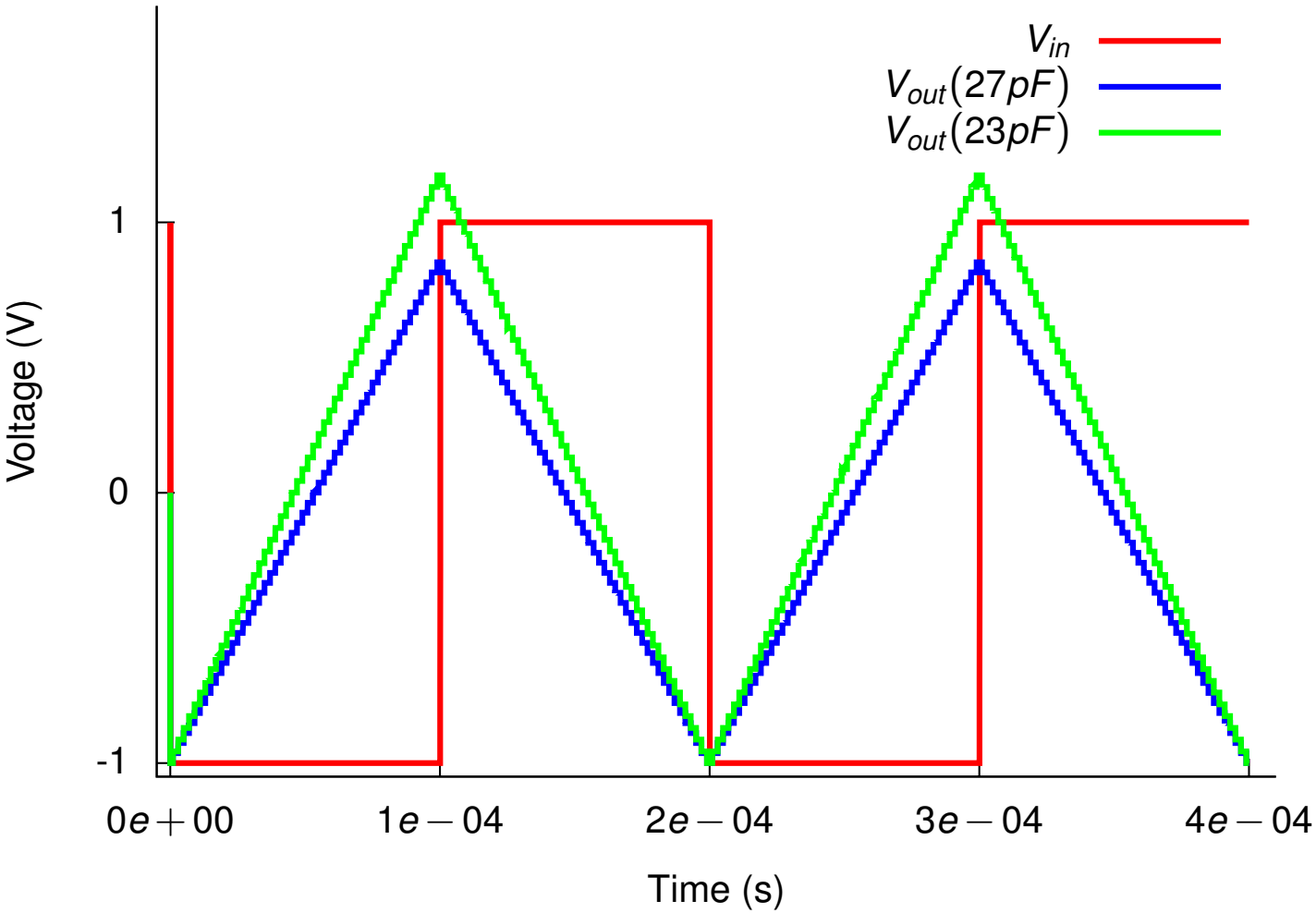
The Case for Analog Circuit Verification



Does V_{out} saturate? (i.e. $-2000mV \leq V_{out} \leq 2000mV$)

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

The Case for Analog Circuit Verification



Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

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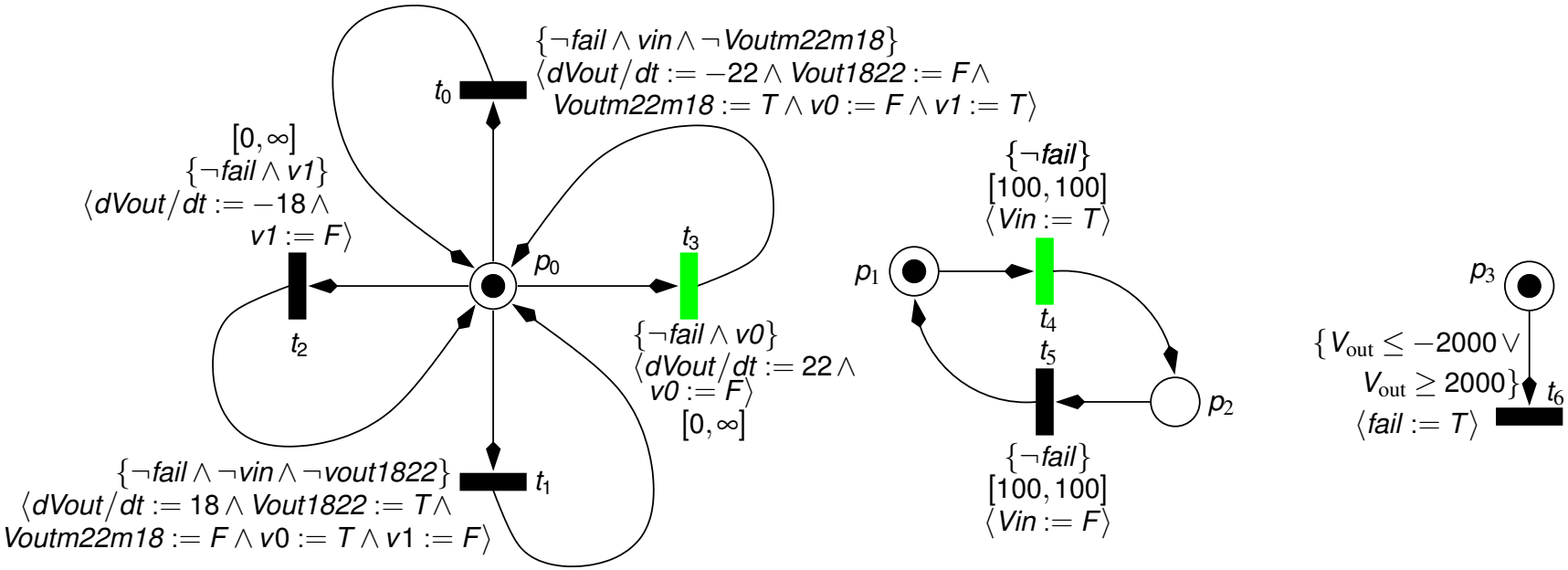


$$c_{t4} = 0$$

$$Vout = -1000mV$$

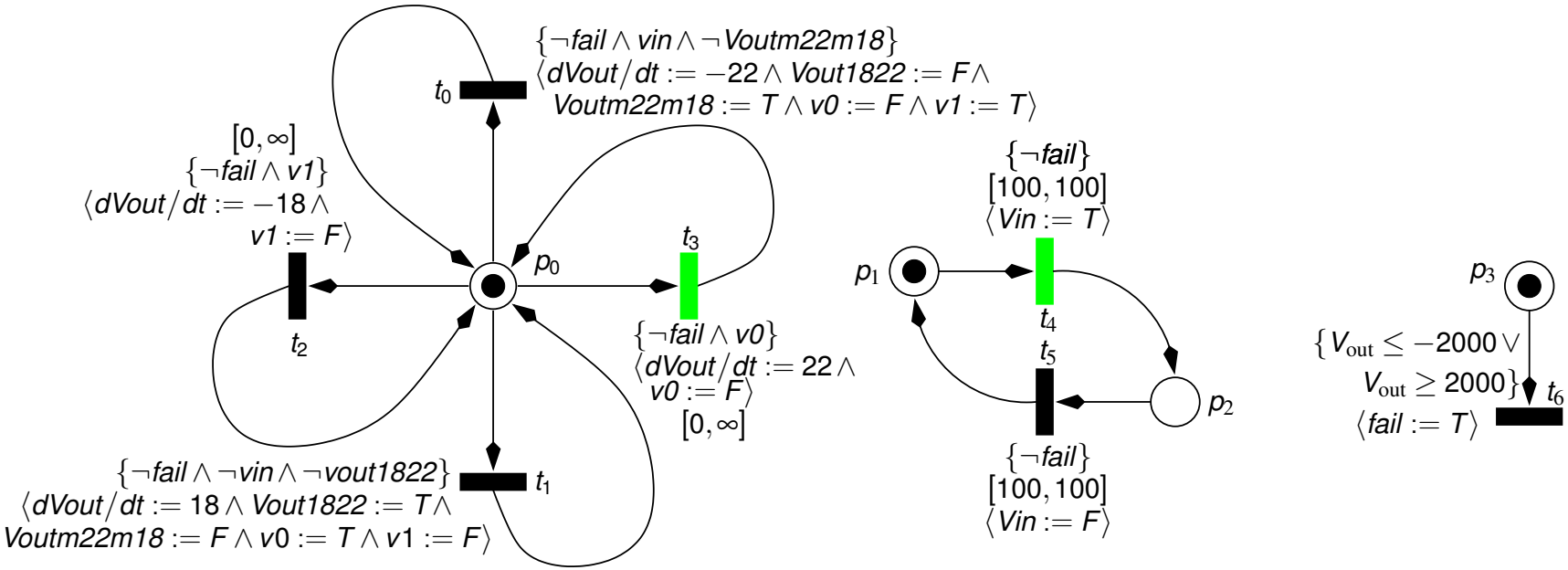
$$dVout/dt = 18mV/\mu s$$

$$vin = \text{F},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$

$$v0 = \text{T},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

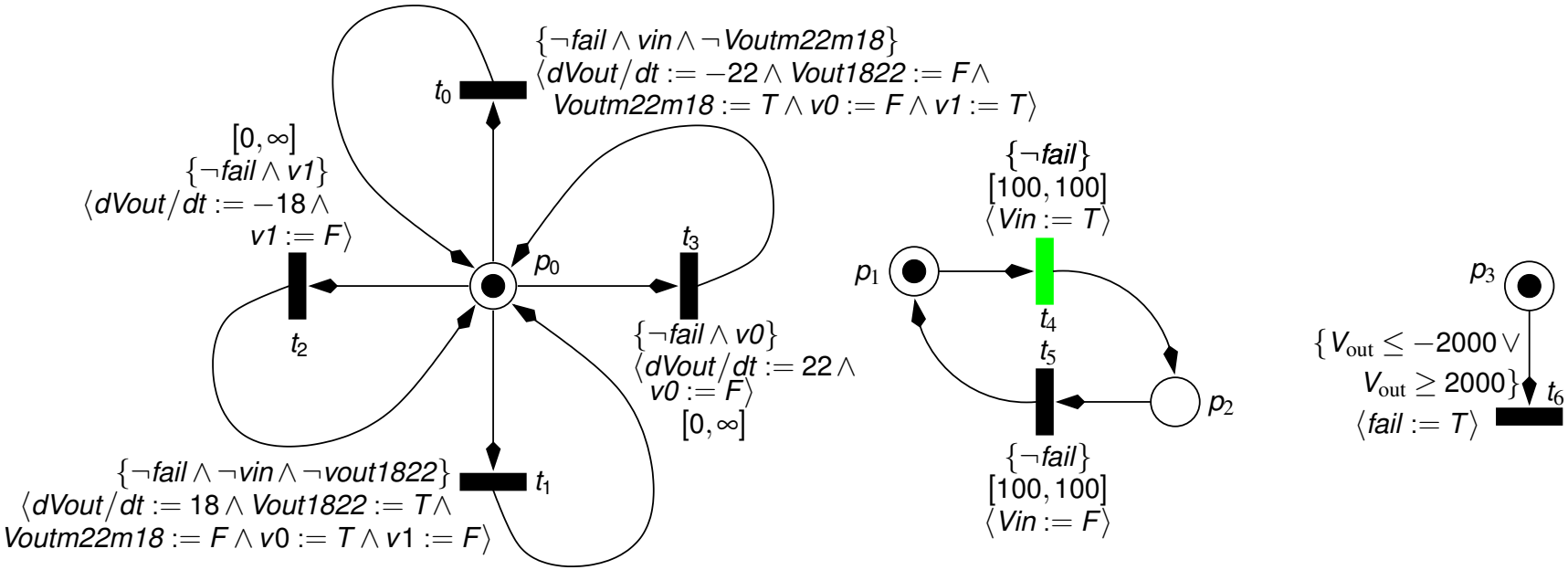
The Case for Analog Circuit Verification



$$0\mu s \leq c_{t4} \leq 100\mu s$$
$$-1000mV \leq Vout \leq 800mV$$
$$dVout/dt = 18mV/\mu s$$
$$vin = \text{F},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$
$$v0 = \text{T},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

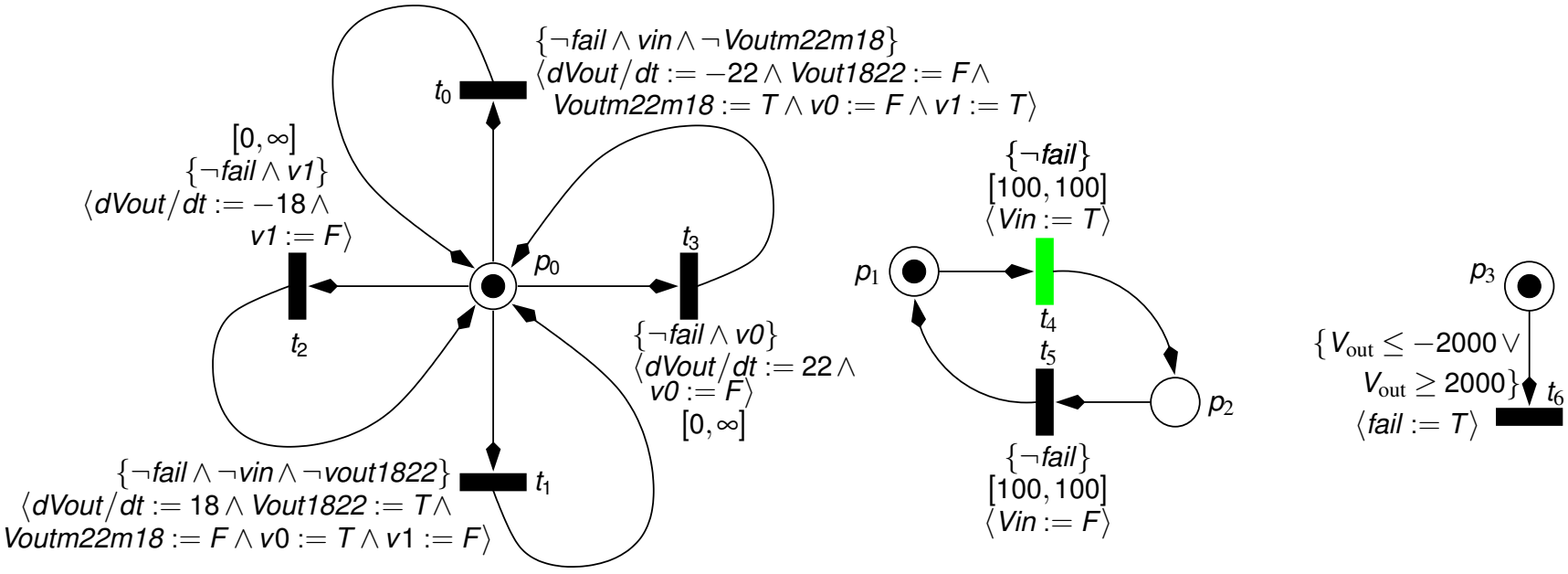
The Case for Analog Circuit Verification



$$0\mu s \leq c_{t4} \leq 100\mu s$$
$$-1000mV \leq Vout \leq 1200mV$$
$$dVout/dt = 22mV/\mu s$$
$$vin = \text{F},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$
$$v0 = \text{F},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

The Case for Analog Circuit Verification



$$c_{t4} = 100\mu s$$

$$800mV \leq Vout \leq 1200mV$$

$$dVout/dt = 22mV/\mu s$$

$$vin = \text{T},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$

$$v0 = \text{F},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

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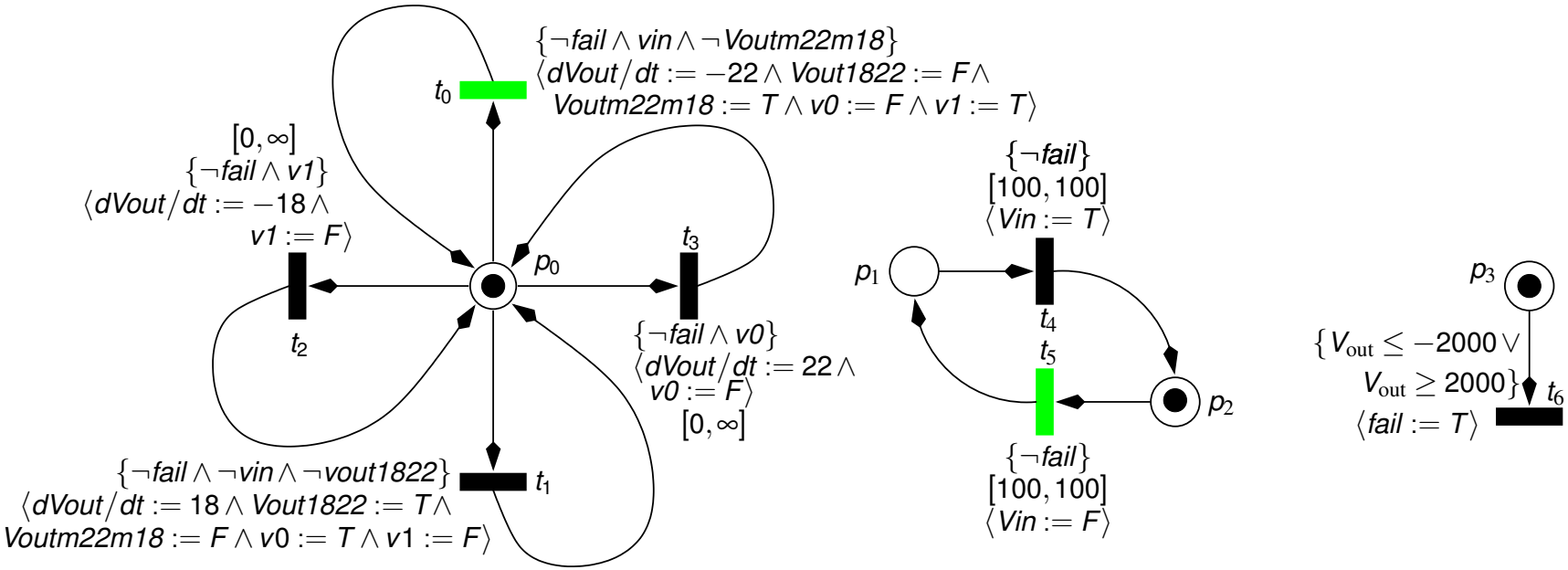
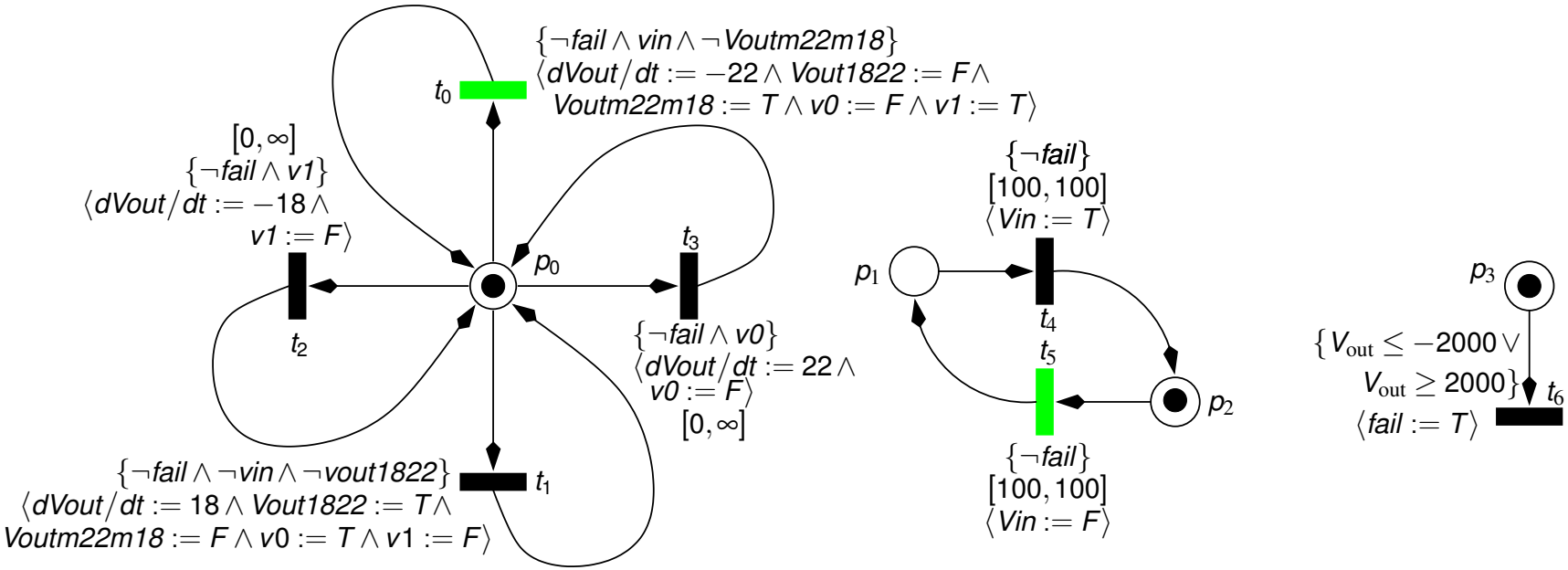


$$c_{t0} = c_{t5} = 0\mu s$$
$$800mV \leq Vout \leq 1200mV$$
$$dVout/dt = 22mV/\mu s$$
$$vin = \text{T},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$
$$v0 = \text{F},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

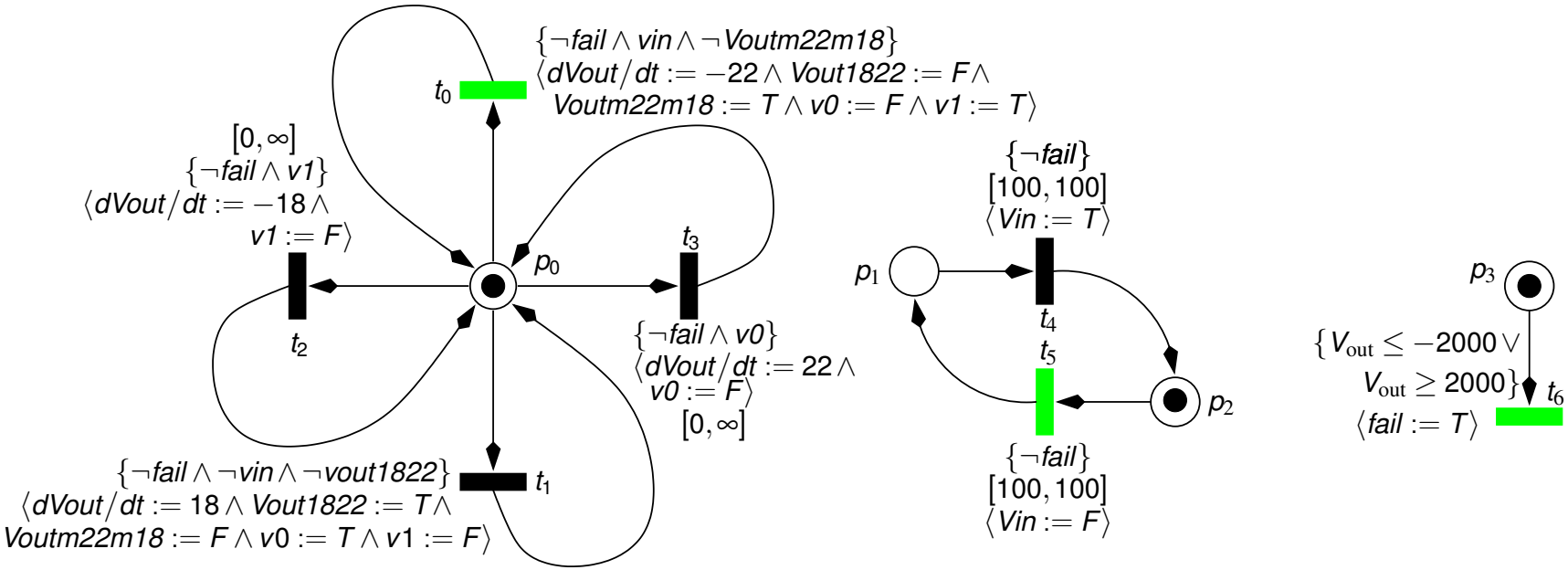
The Case for Analog Circuit Verification



$$c_{t0} = c_{t5} = 0\mu s$$
$$400mV \leq Vout \leq 1600mV$$
$$dVout/dt = 22mV/\mu s$$
$$vin = \text{T},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$
$$v0 = \text{F},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

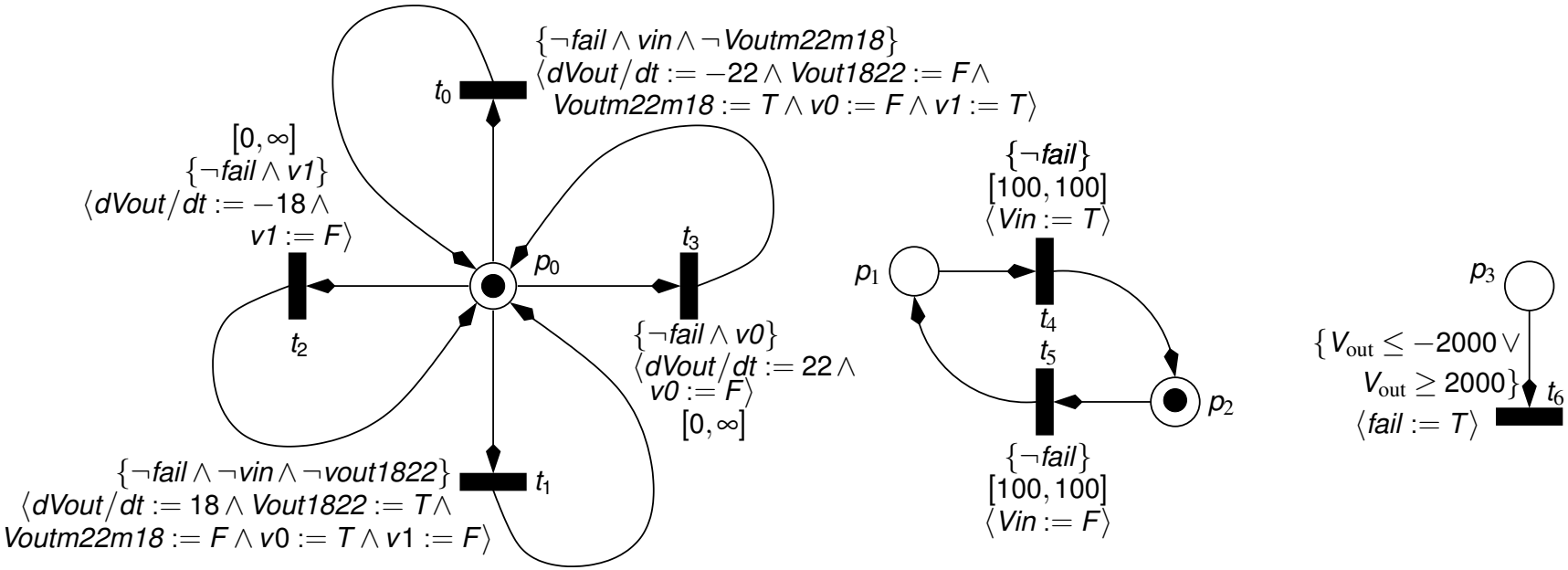
The Case for Analog Circuit Verification



$$c_{t0} = c_{t5} = c_{t6} = 0\mu s$$
$$0mV \leq Vout \leq 2000mV$$
$$dVout/dt = 22mV/\mu s$$
$$vin = \text{T},\ Vout1822 = \text{T},\ Voutm22m18 = \text{F},$$
$$v0 = \text{F},\ v1 = \text{F},\ fail = \text{F}$$

Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

The Case for Analog Circuit Verification



DEADLOCK

$$0mV \leq Vout \leq 2000mV$$

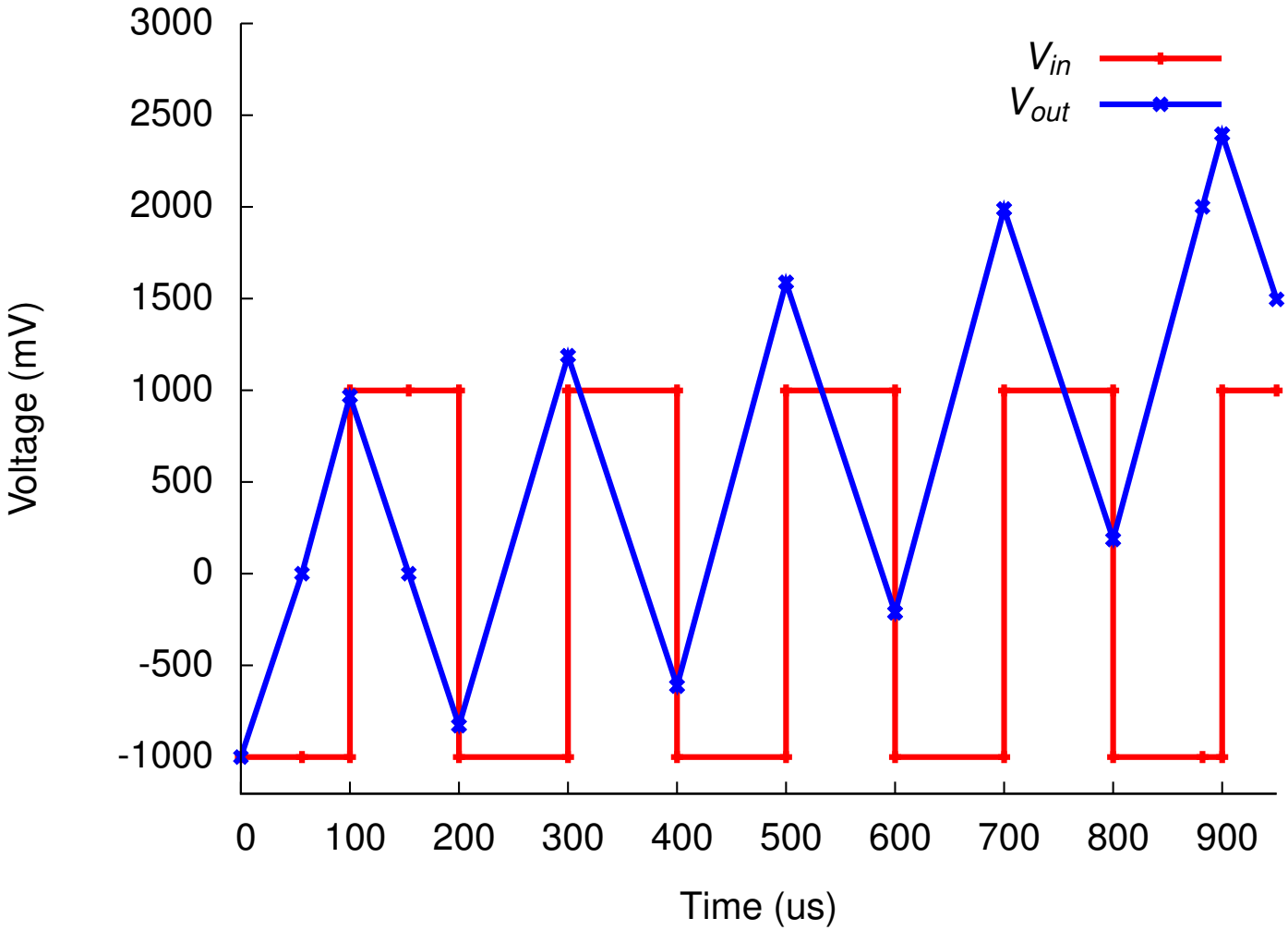
$$dVout/dt = 22mV/\mu s$$

vin = T, $Vout1822$ = T, $Voutm22m18$ = F,

$v0$ = F, $v1$ = F, $fail$ = T

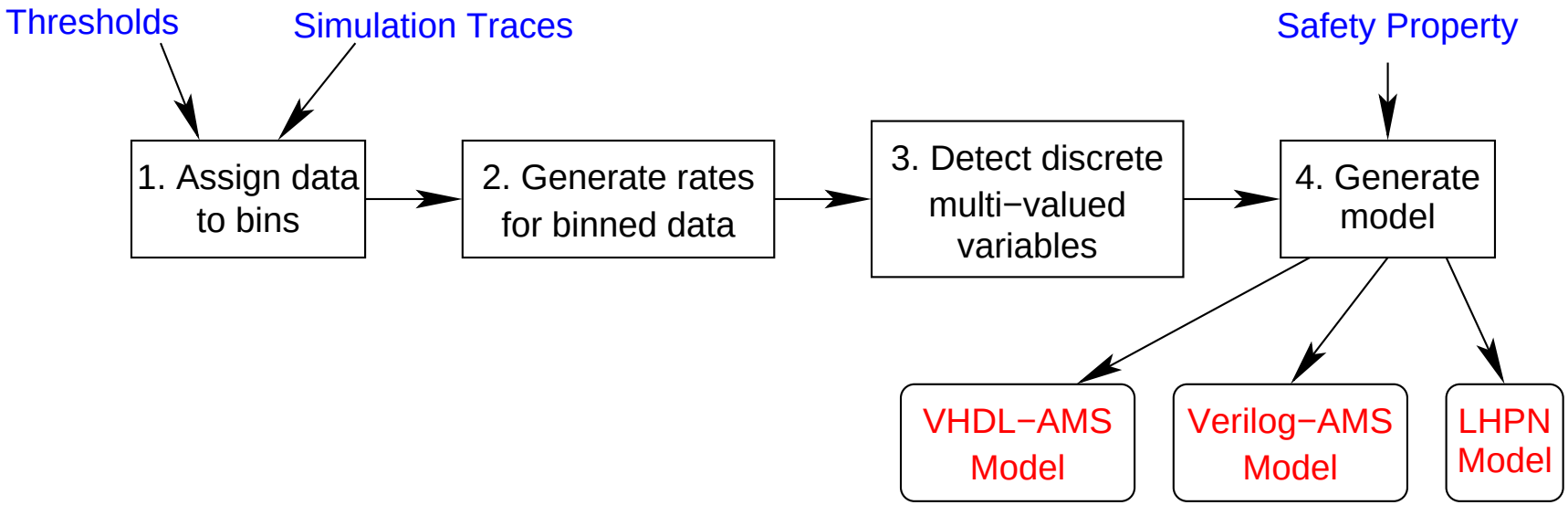
Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

The Case for Analog Circuit Verification



Myers et al., Edinburgh, UK, Formal Verif. of Analog Circuits (FAC), 2005.

Simulation Aided Verification of AMS Circuits



Little et al., Princeton, USA, Formal Verification of Analog Circuits (FAC) 2008.

FAC 2009 Grenoble, France

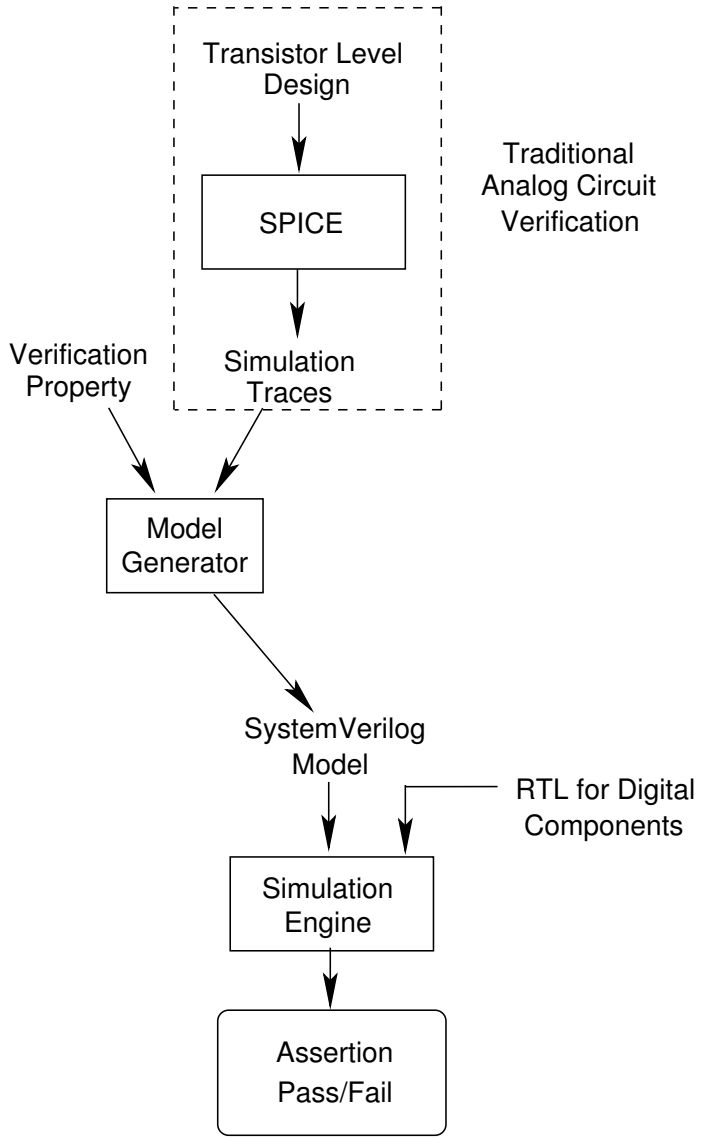
Formal Verification of Analog Circuits (FAC) '09

A satellite workshop of CAV 2009

June 26, 2009, Grenoble, France

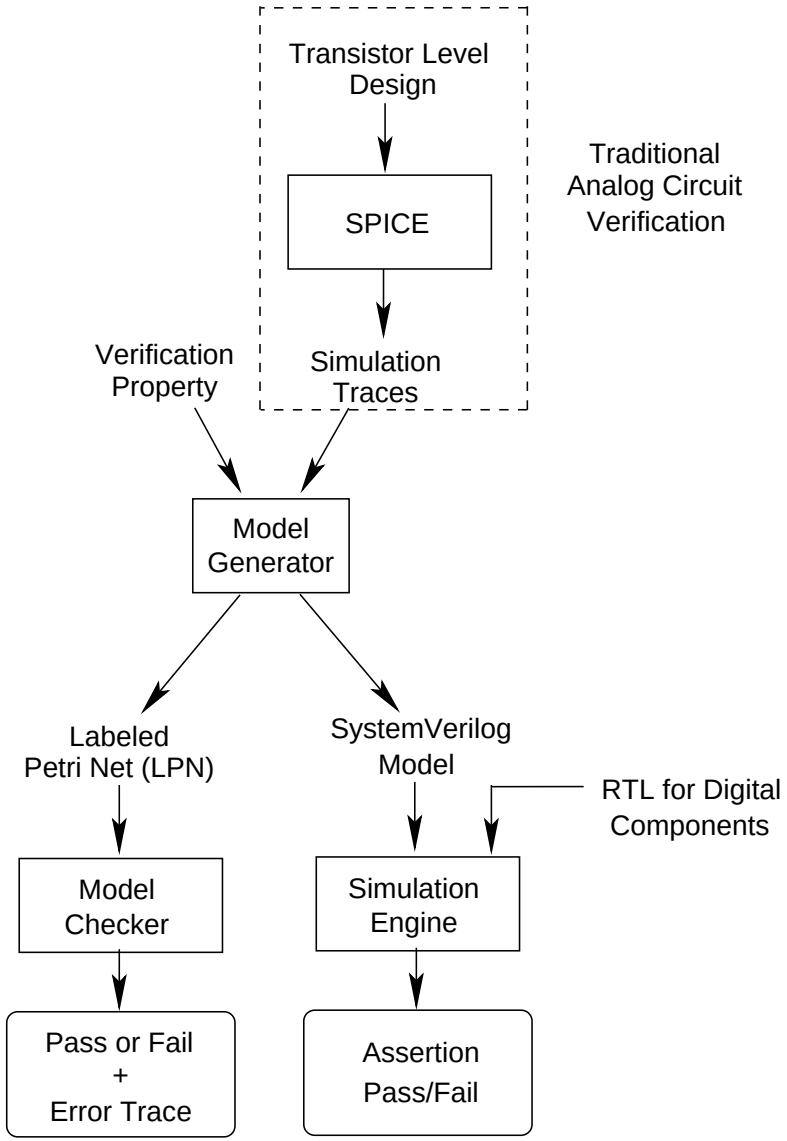
Organizers: Goran Frehse and Lars Hedrich

Automatic Generation of Abstract Models for AMS Circuits



Batchu, et al., Salt Lake City, USA, Frontiers in Analog CAD (FAC) 2011.

Automatic Generation of Abstract Models for AMS Circuits



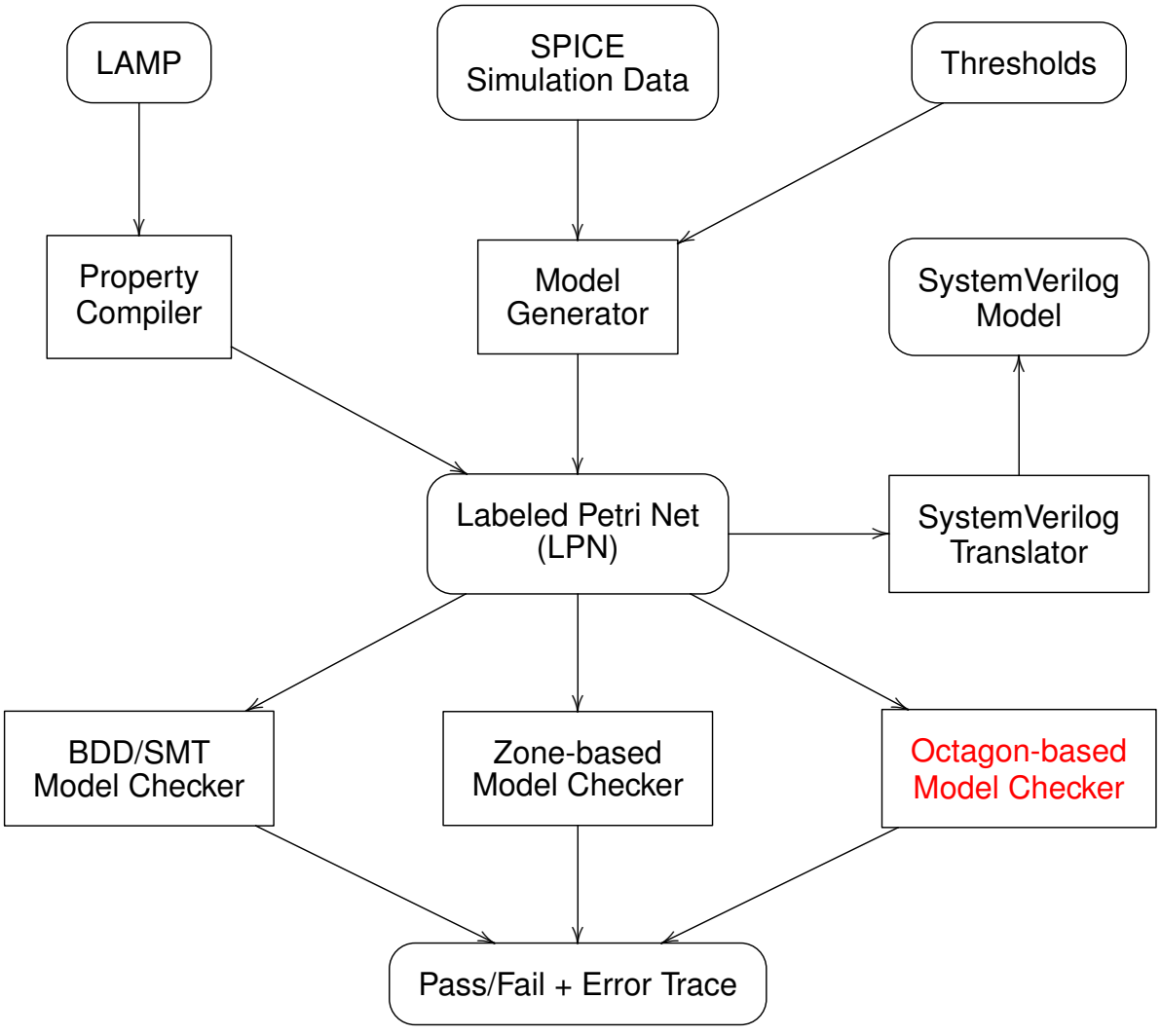
Batchu, et al., Salt Lake City, USA, Frontiers in Analog CAD (FAC) 2011.

A New Assertion Property Language for AMS Circuits

```
property PhaseInterpolator {
  real ctl, omega, phi;
  always{
    wait(phi >= 0);
    if (ctl = 1) {
      assert(omega < 2.2, 1375);
      wait(omega >= 2.2, 10);
    } else if (ctl = 2) {
      assert(omega < 2.2, 1315);
      wait(omega >= 2.2, 10);
    } else if (ctl = 3) {
      assert(omega < 2.2, 1255);
      wait(omega >= 2.2, 10);
    }
    wait(phi < 0);
  }
}
```

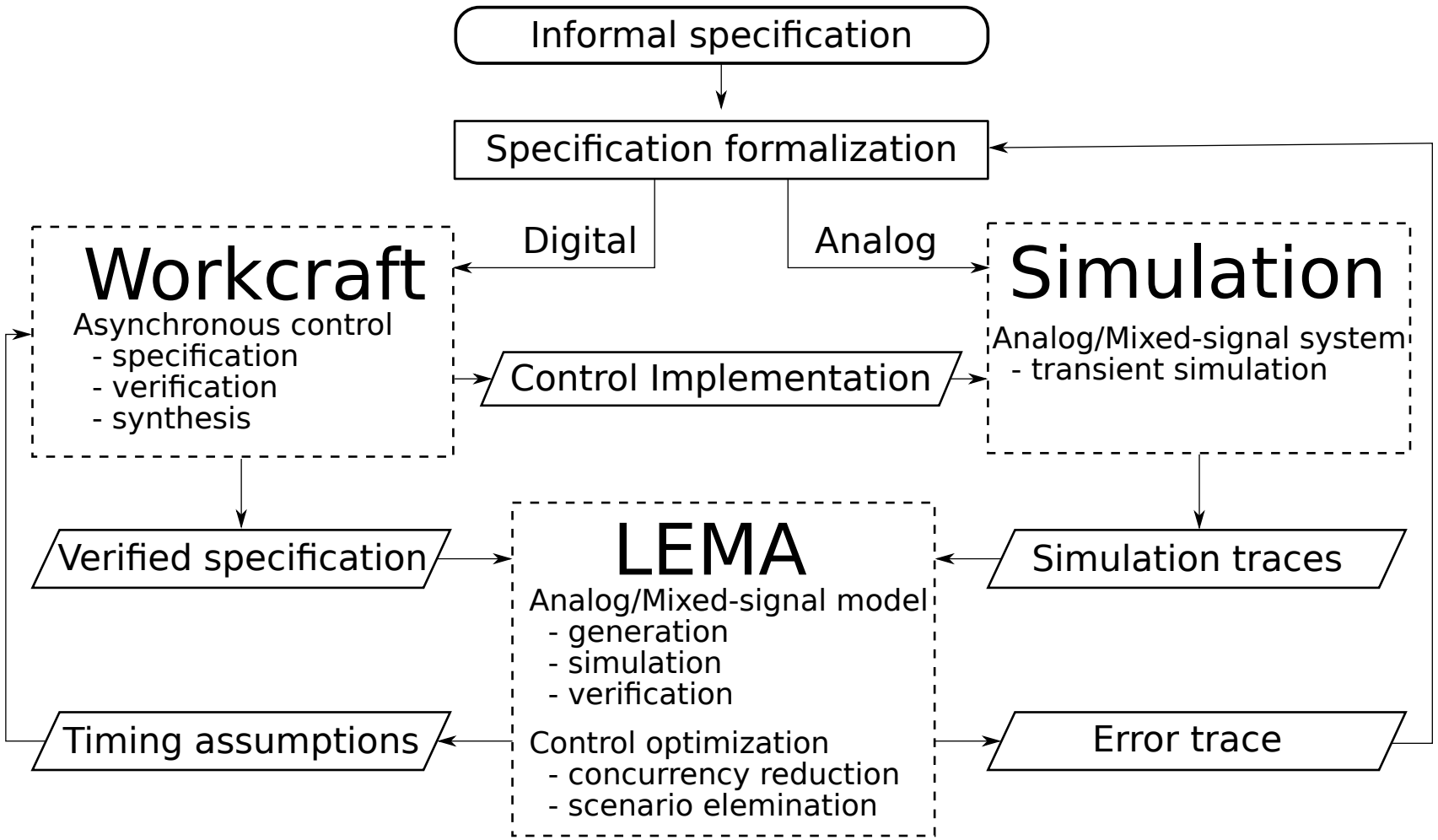
Kulkarni, et al., Berkeley, USA, Frontiers in Analog CAD (FAC) 2013.

Reachability Analysis Using Octagons



Fisher, et al., Grenoble, France, Frontiers in Analog CAD (FAC) 2014.

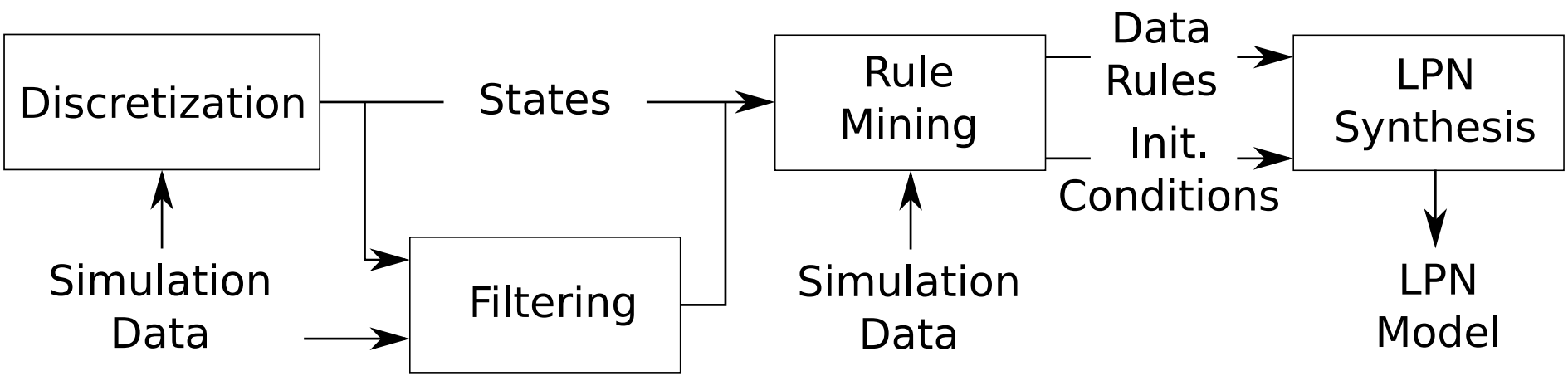
A Workflow for the Design of Mixed-signal Systems with Asynchronous Control



Dubikhin, et al., Austin, USA, Frontiers in Analog CAD (FAC) 2015.

Dubikhin et al., IEEE Design & Test, 2016.

Model Discovery for Analog/Mixed-Signal Circuits



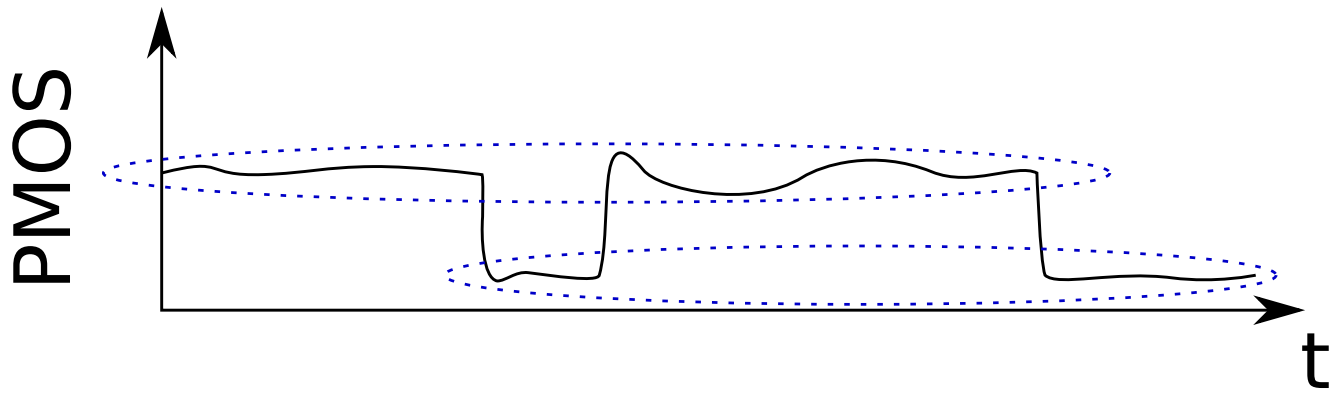
Dubikhin, et al., Frankfurt, Germany, Frontiers in Analog CAD (FAC) 2017.

Today's talk:

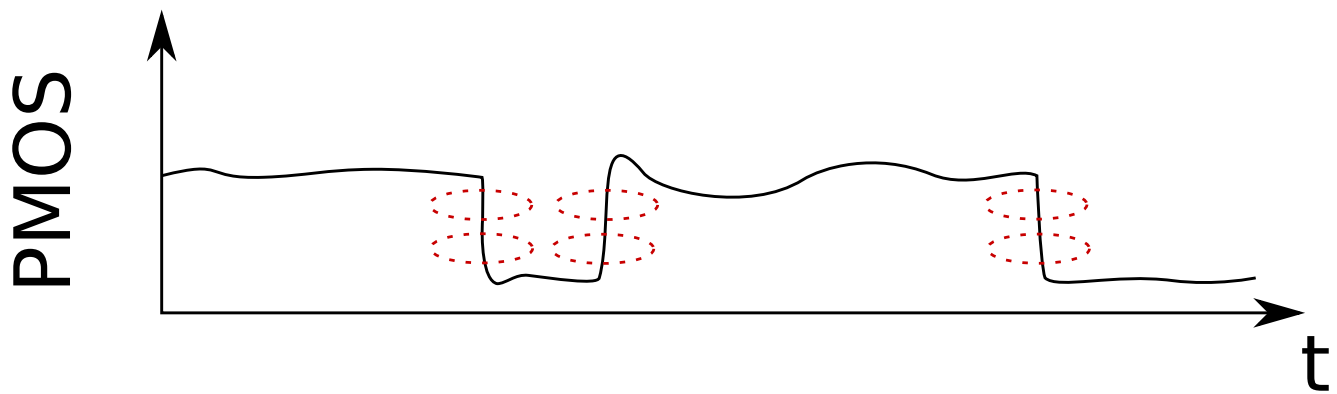
- New project architecture with metric functions
- Improved DMV discretization method based on data clusterization
- New adaptive low pass filter for states filtering

DMV Discretization

- Form dendrogram from data values
- Create a set of clusters using relative standard deviation

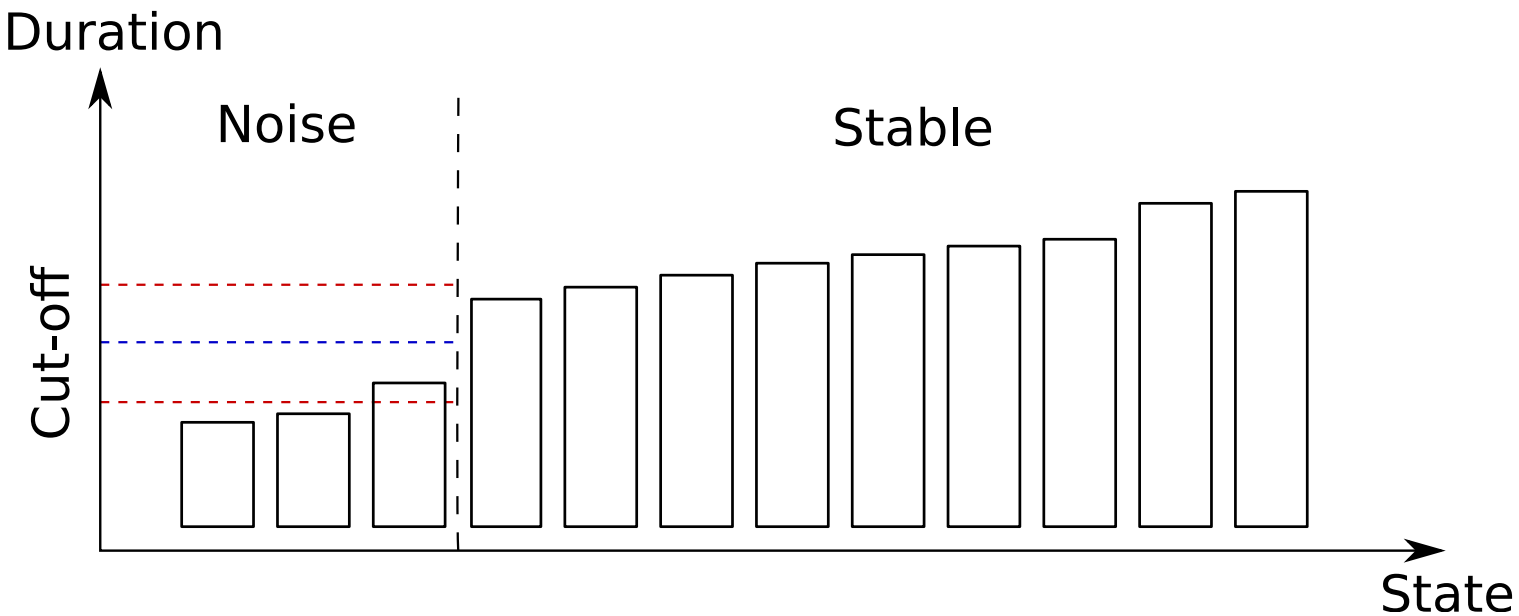


- Perform preliminary discretization of data
- Detect low duration states and remove transient clusters



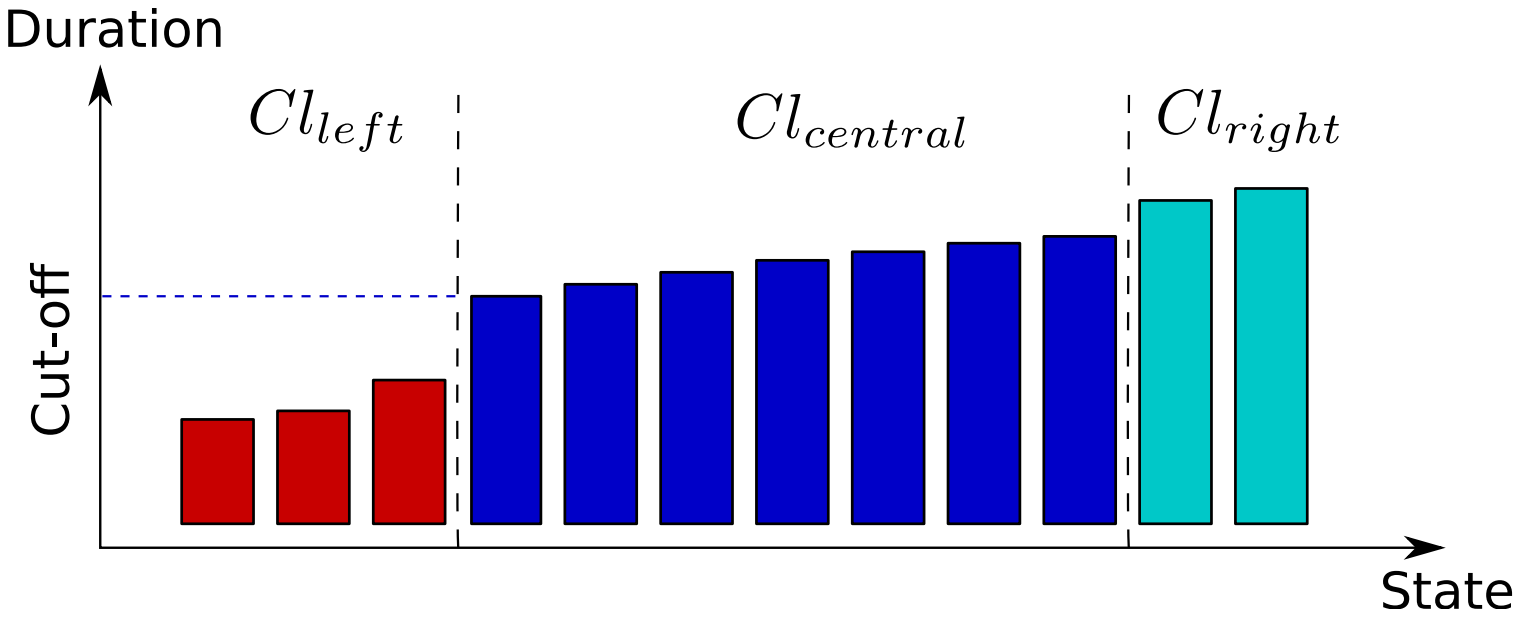
Fixed Low Pass Filter

- The cut-off threshold has to be manually selected
- Noise states preserved or stable states removed

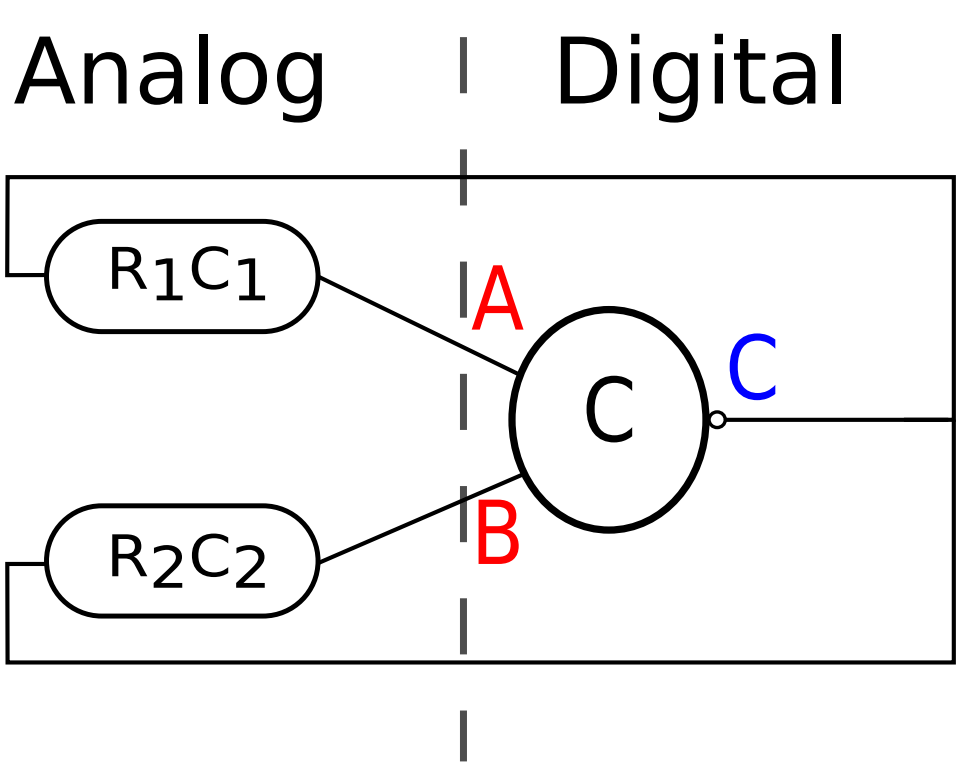


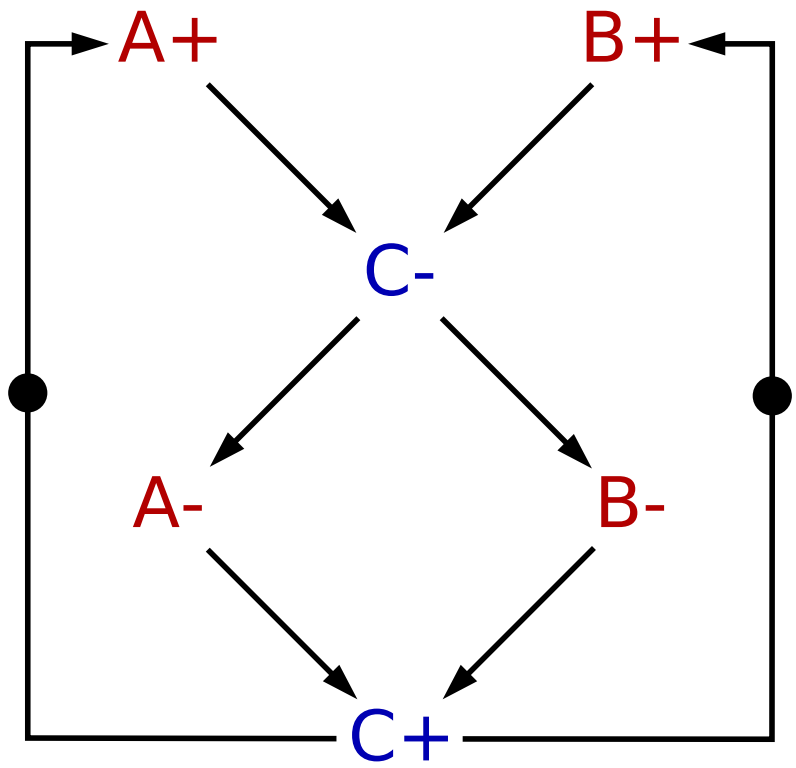
Adaptive Low Pass Filter

- Use agglomerative clustering to group states by their duration
- Find a composition of clusters based on relative duration
- Select cut-off as minimum duration state in the largest cluster

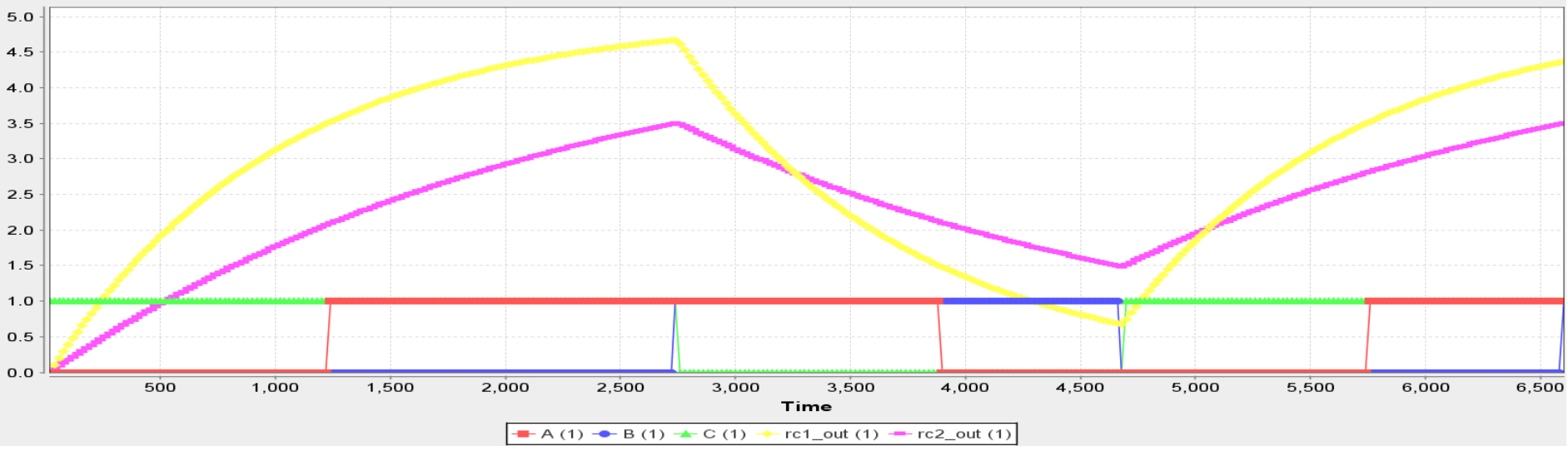


C-element Example



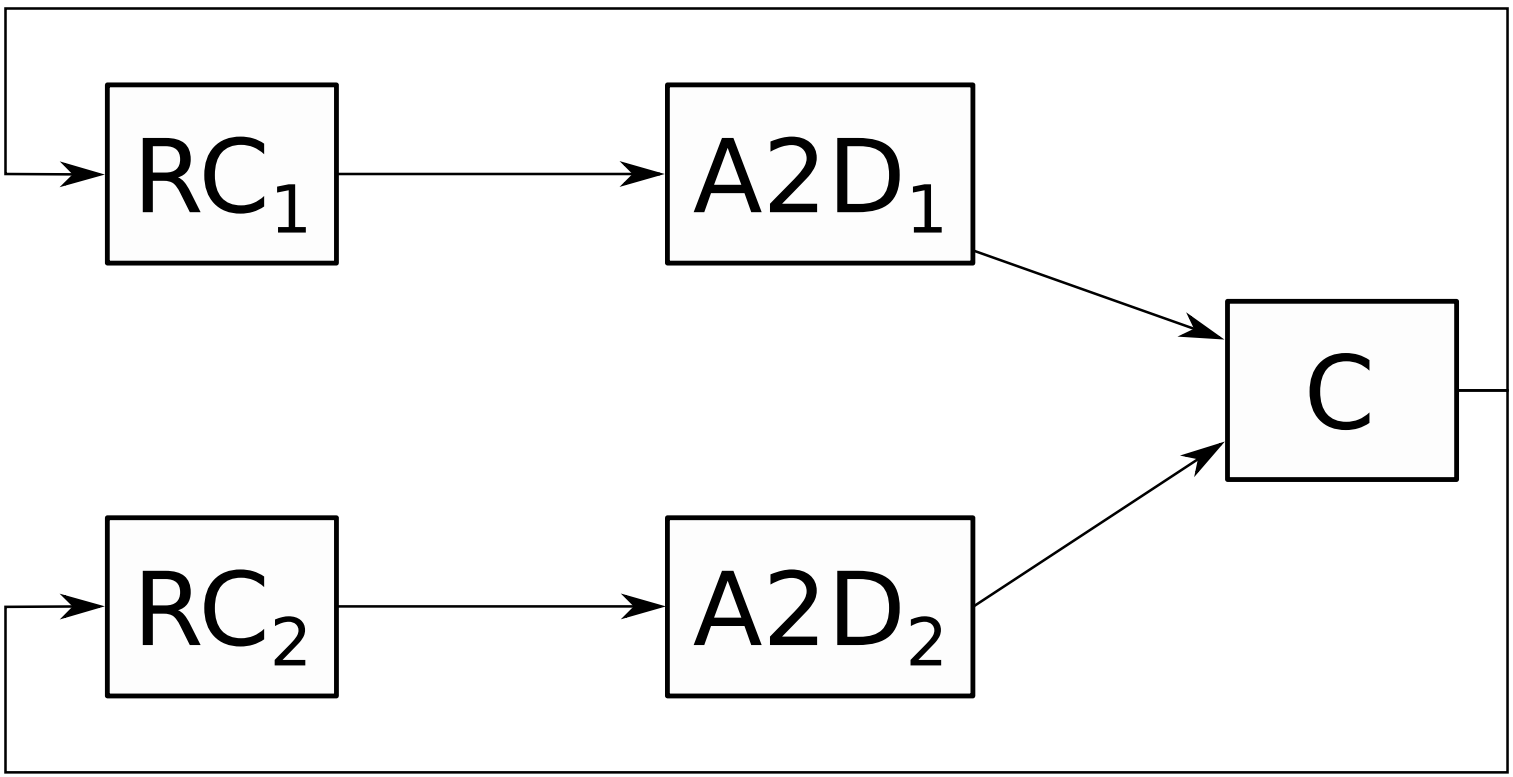


C-element Simulation Waveform



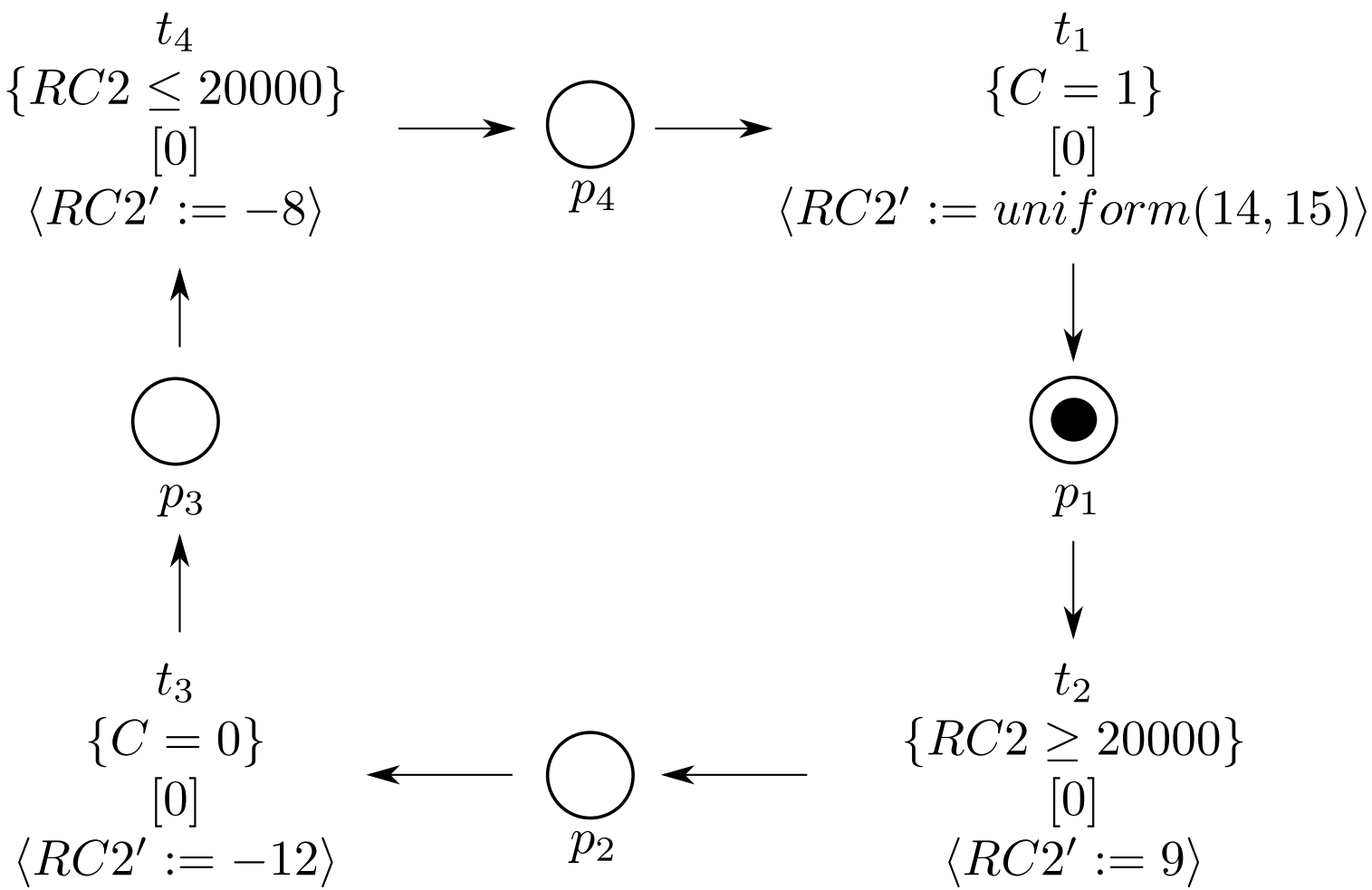
C-element Model

- Every component is modeled individually
- C-element is converted from STG to LPN
- Explicit A2D modules are created

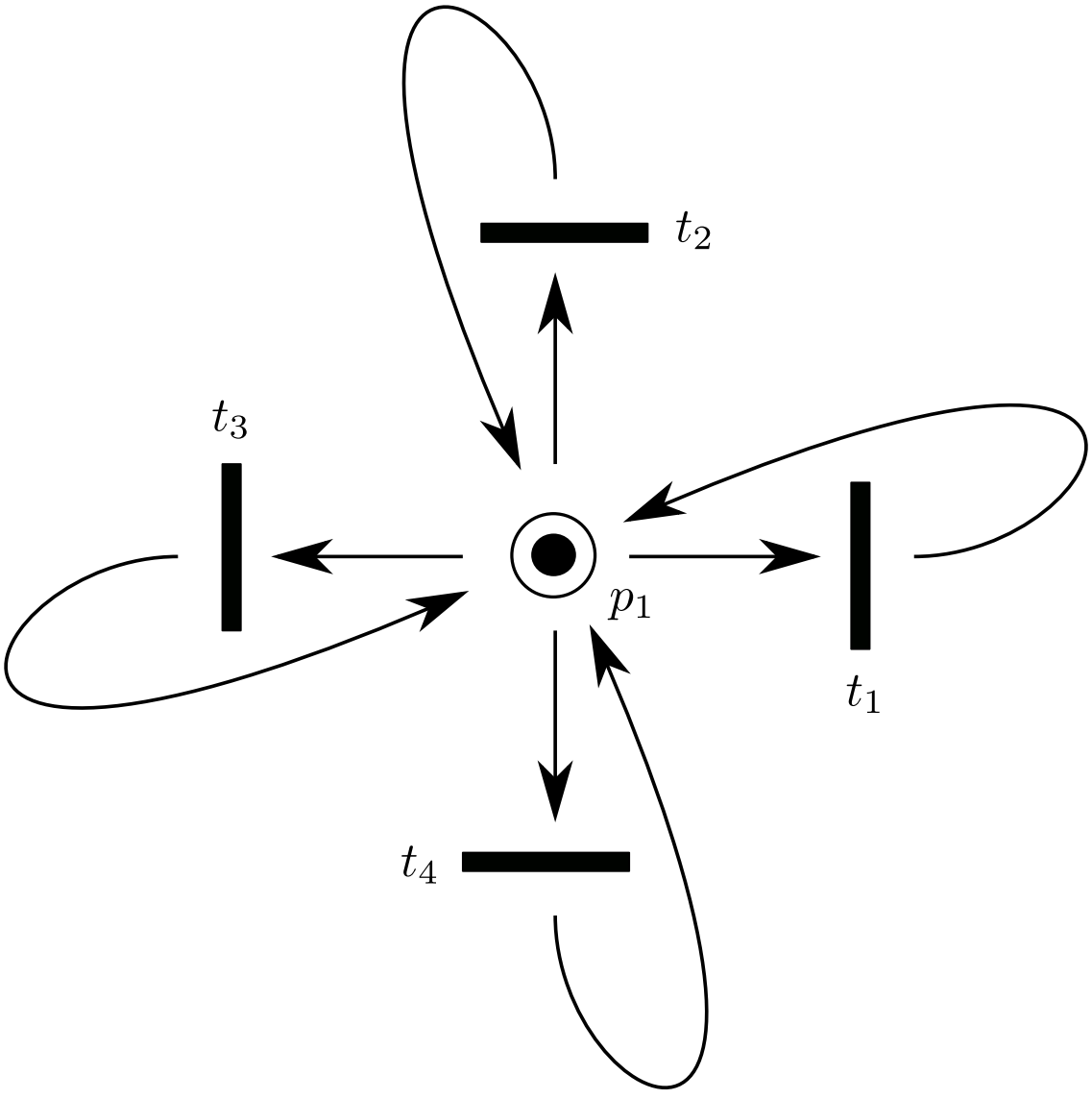


RC Original Model

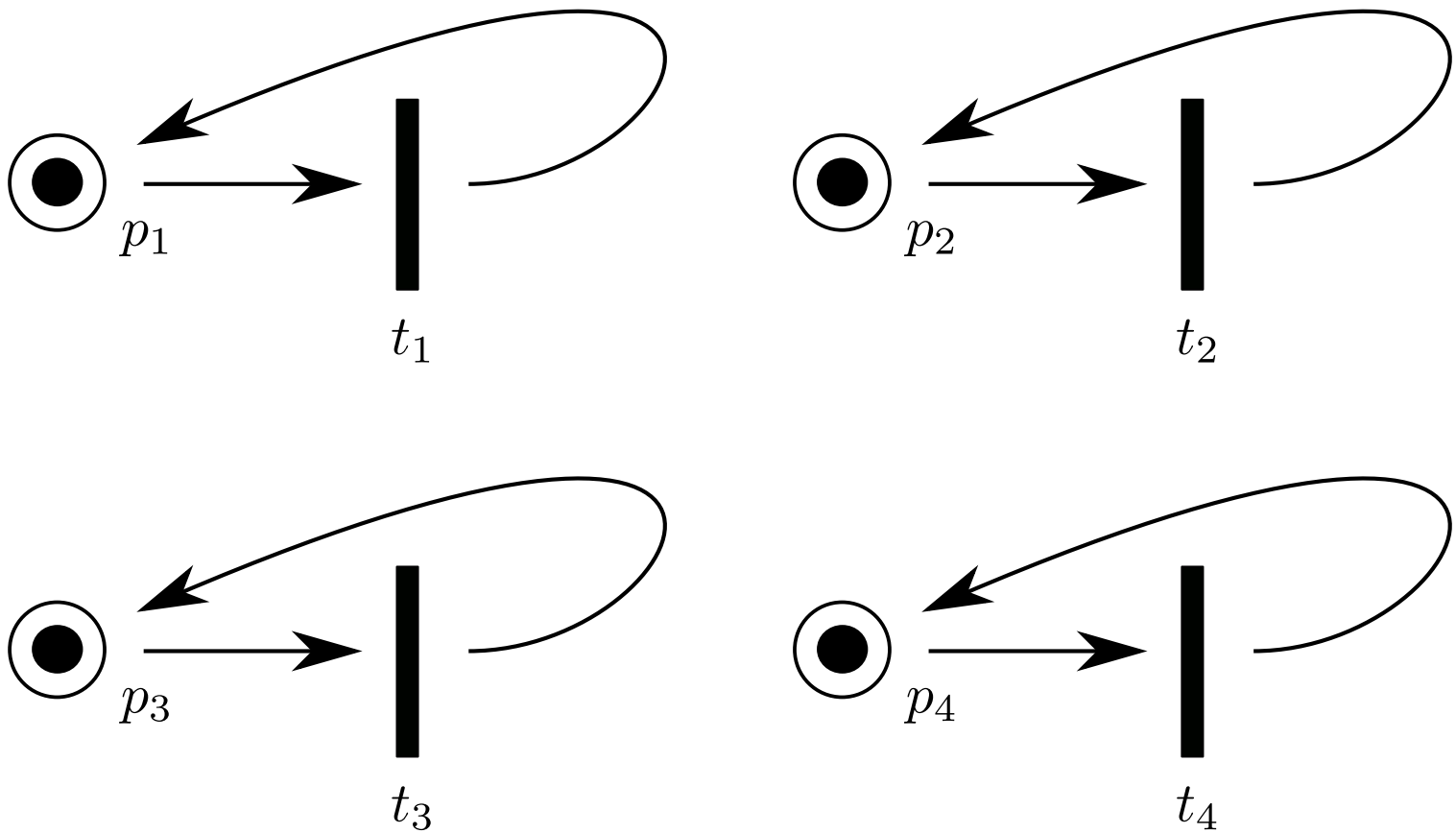
$RC2 := 0$
$RC2\_rate := uniform(14, 15)$



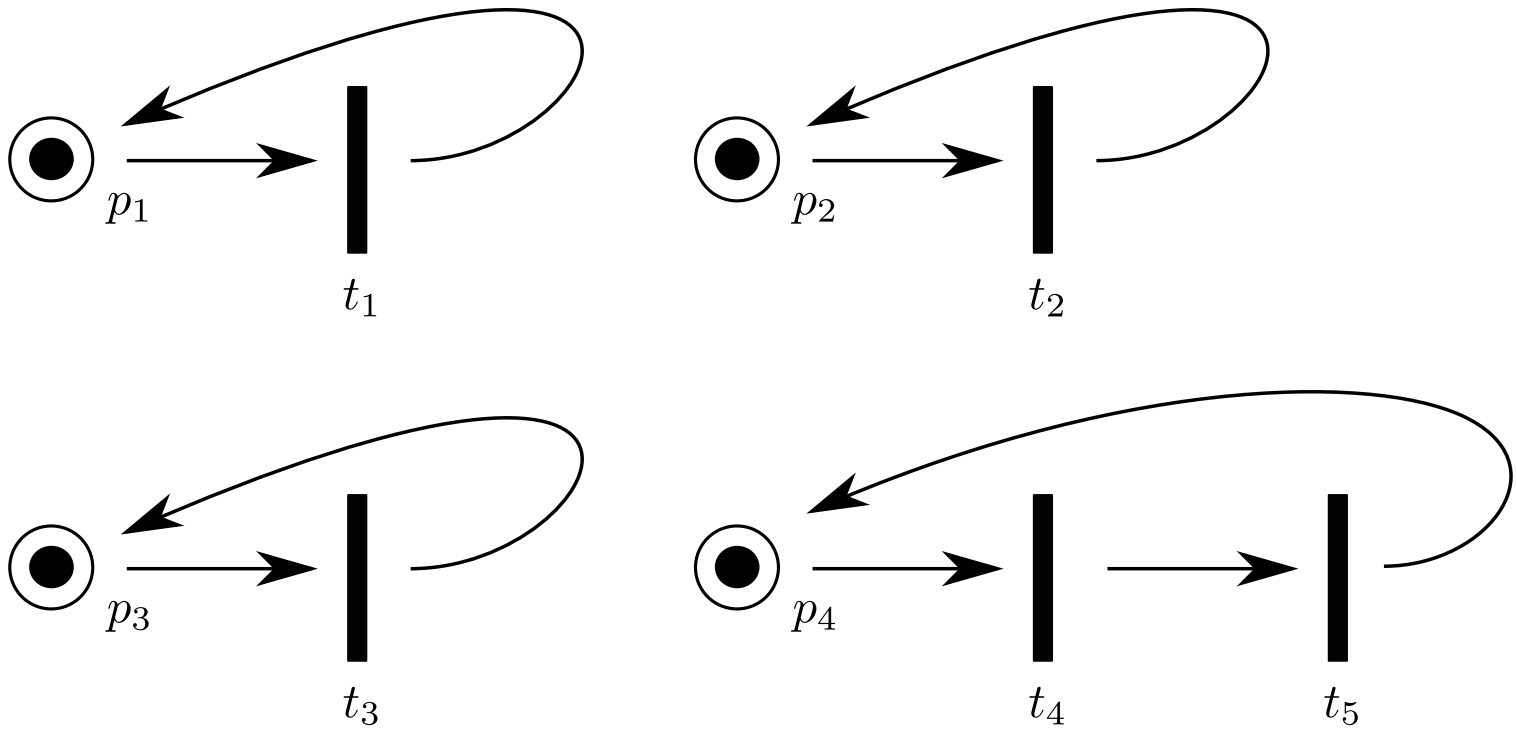
Flower Model



Flower Model Decomposed



Flower Model Decomposed Extended

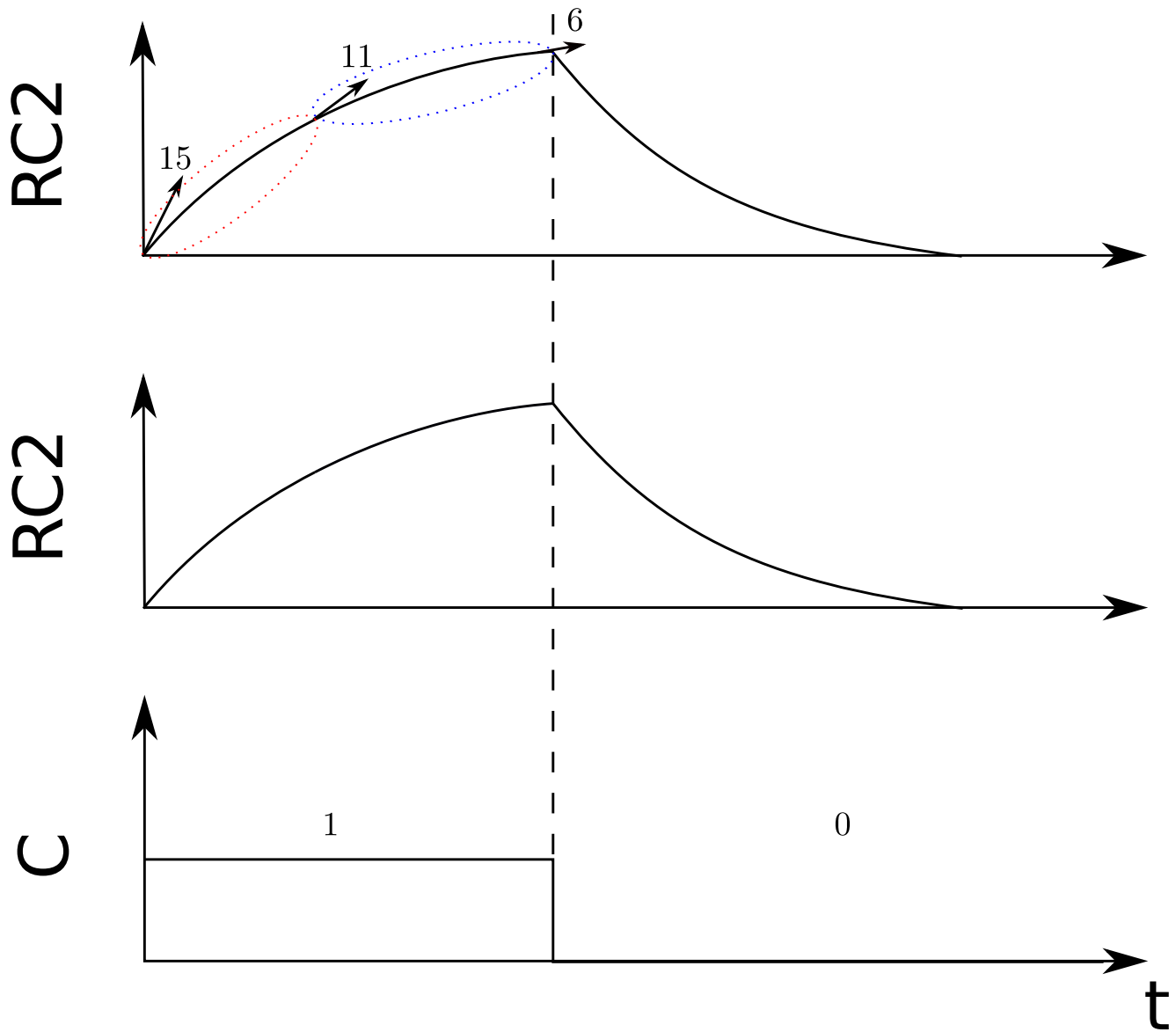


Rule Mining

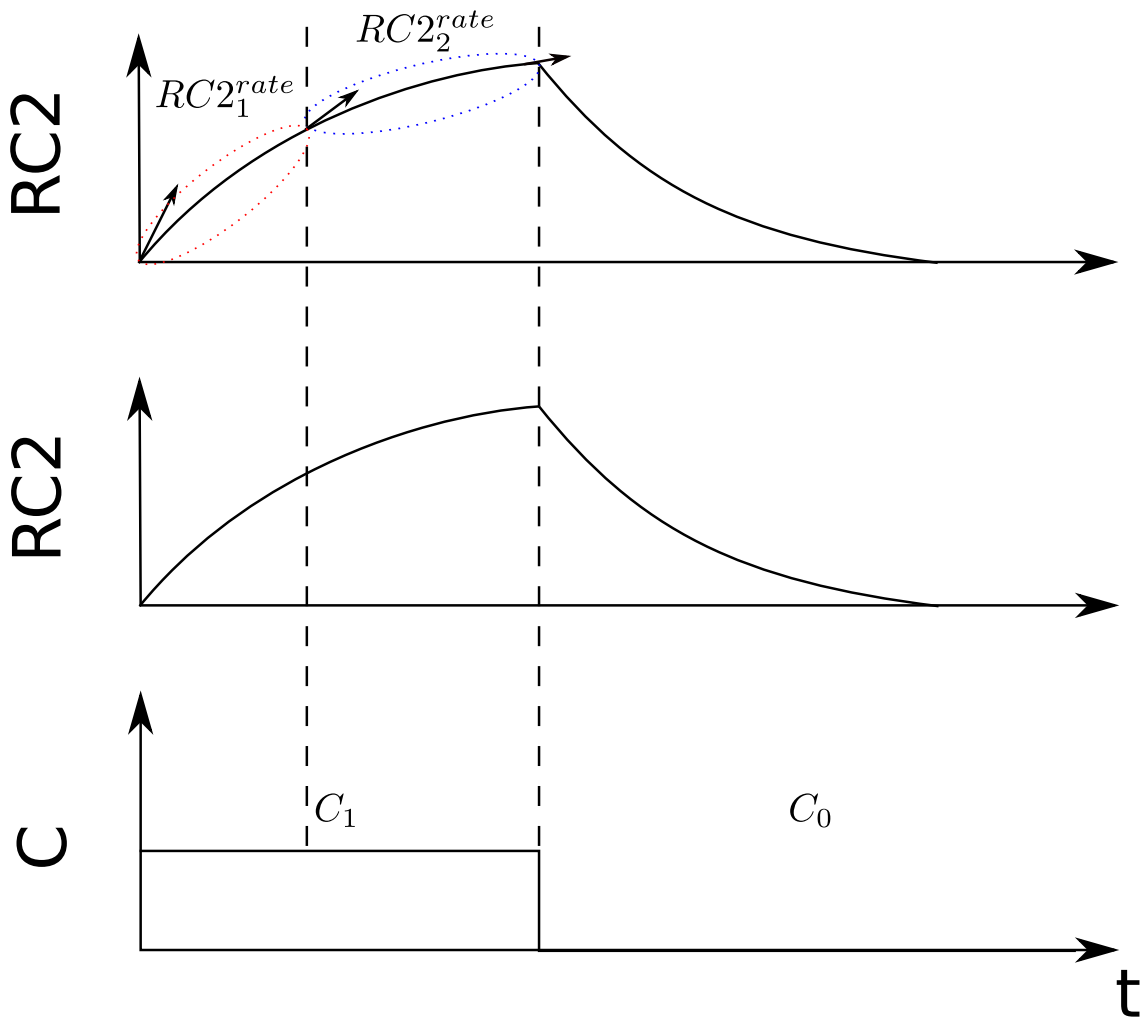
Rules are relations between the control state sequences and the output states.

- Extract data patterns (DP) for output from state traces
  - Pattern is a sequence of input states before output change
- Calculate a set of rule patterns (RP) for output states
  - Rule pattern is a surjective function
  - Rule pattern is the min-set of data pattern

RC Improved Model Construction



RC Improved Model Construction

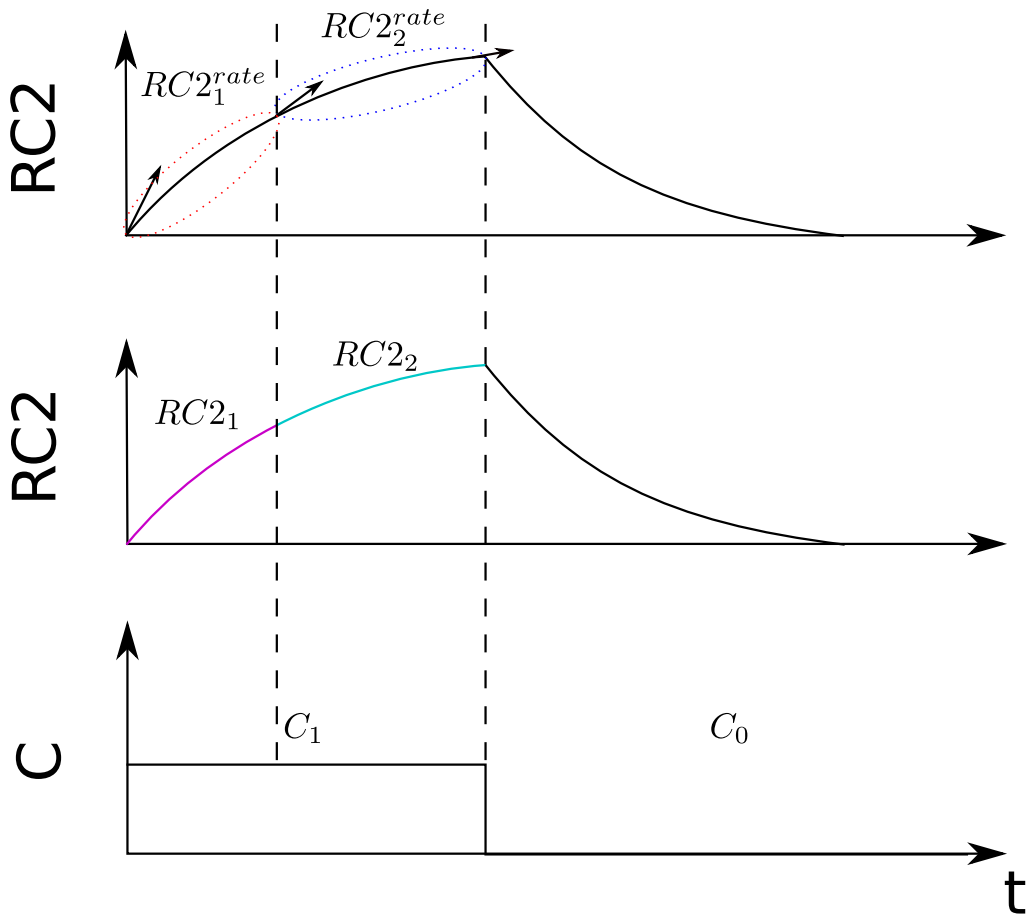


RP

$RC2_1^{rate} : \langle C_1 \rangle$

$RC2_2^{rate} : \langle C_1 \rangle$

RC Improved Model Construction

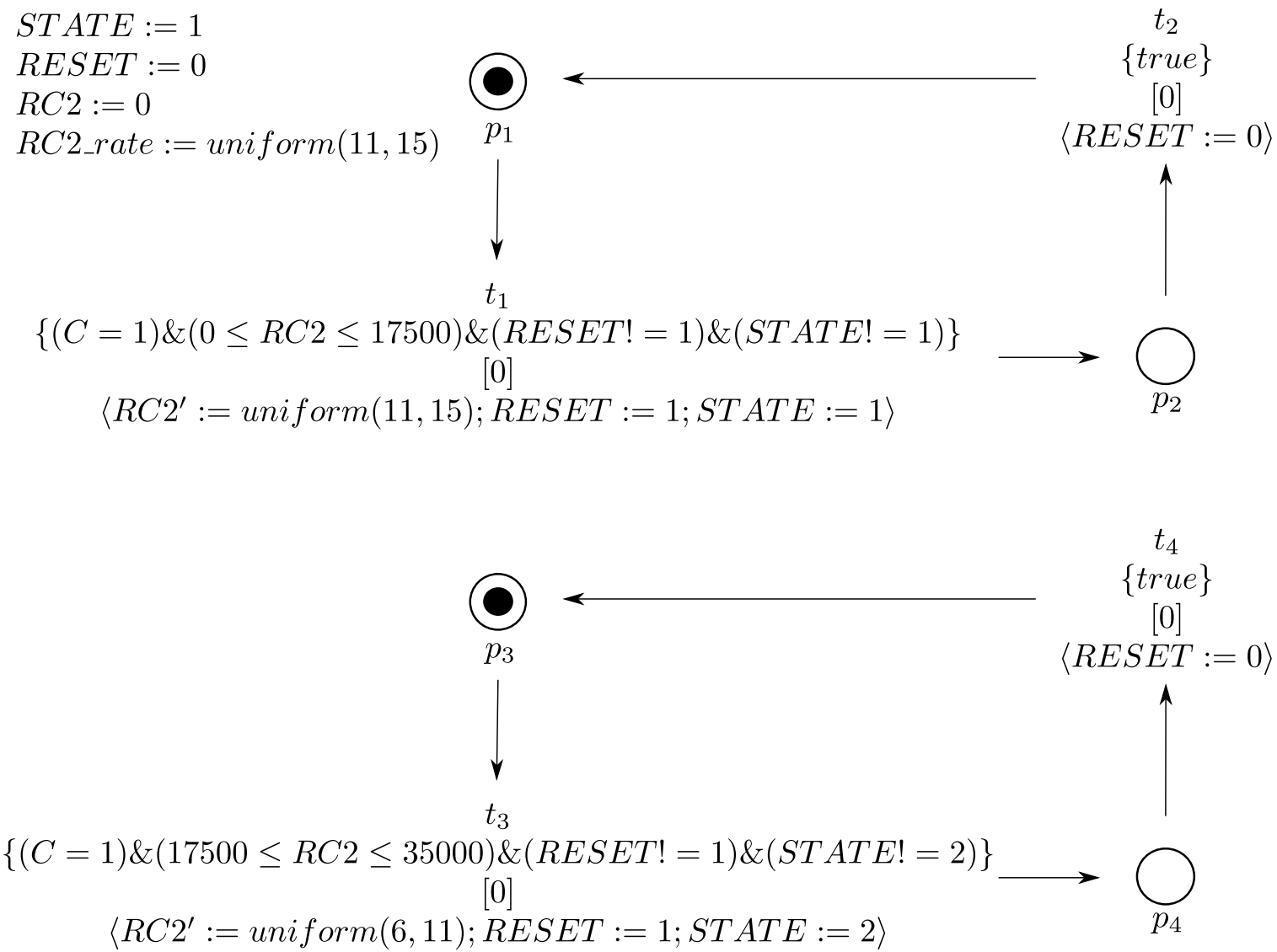


RP

$$RC2_1^{rate} : \langle RC2_1, C_1 \rangle$$

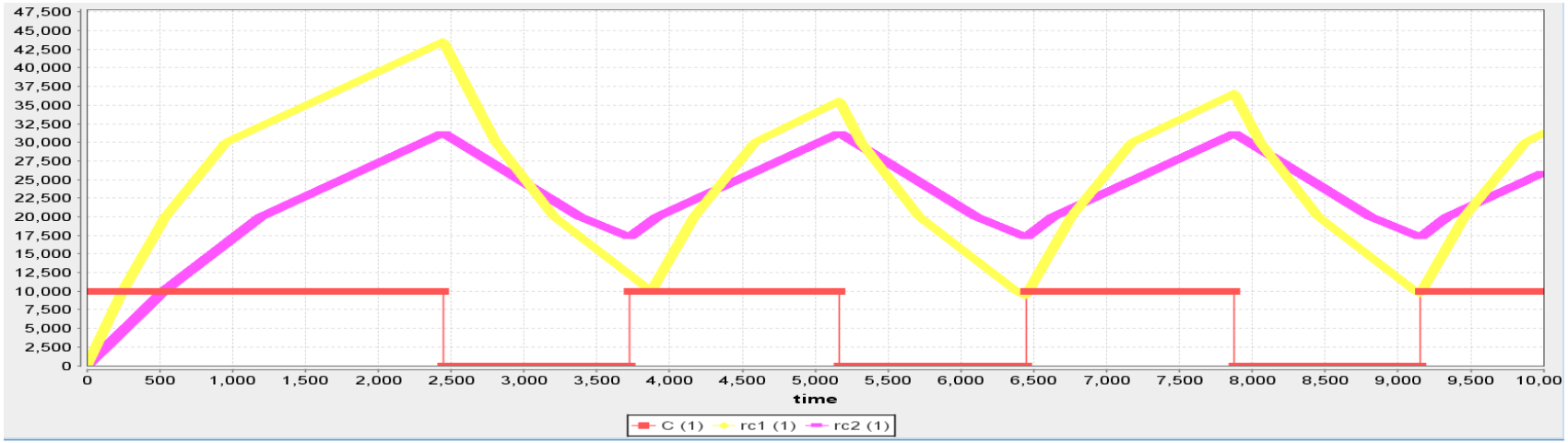
$$RC2_2^{rate} : \langle RC2_2, C_1 \rangle$$

RC Improved Model

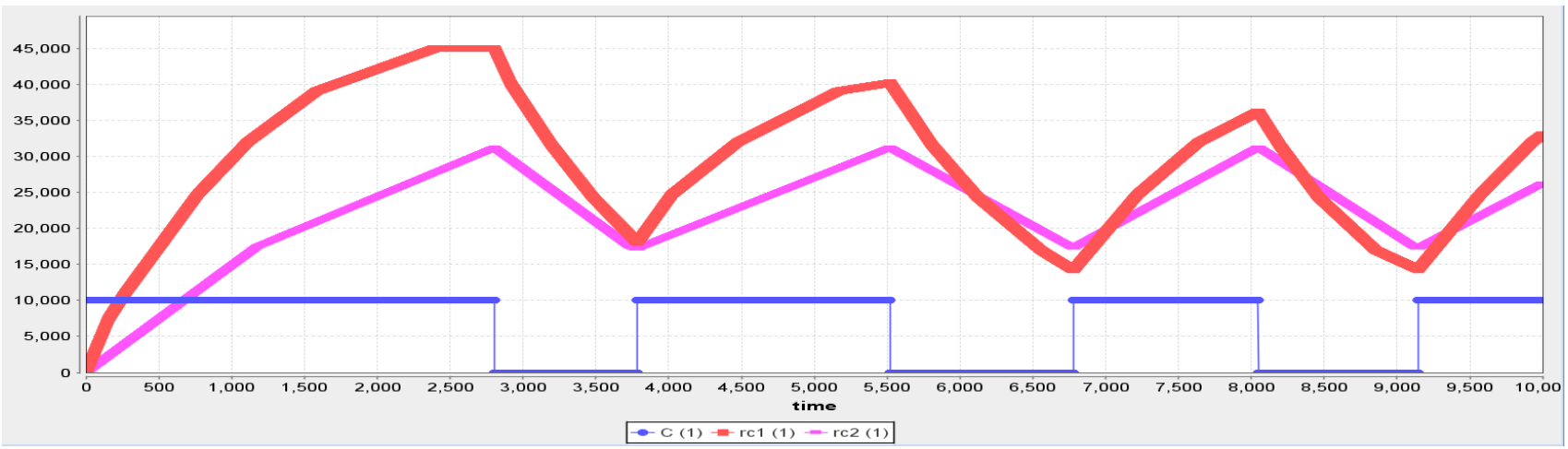


C-element Model Simulation

- Original model

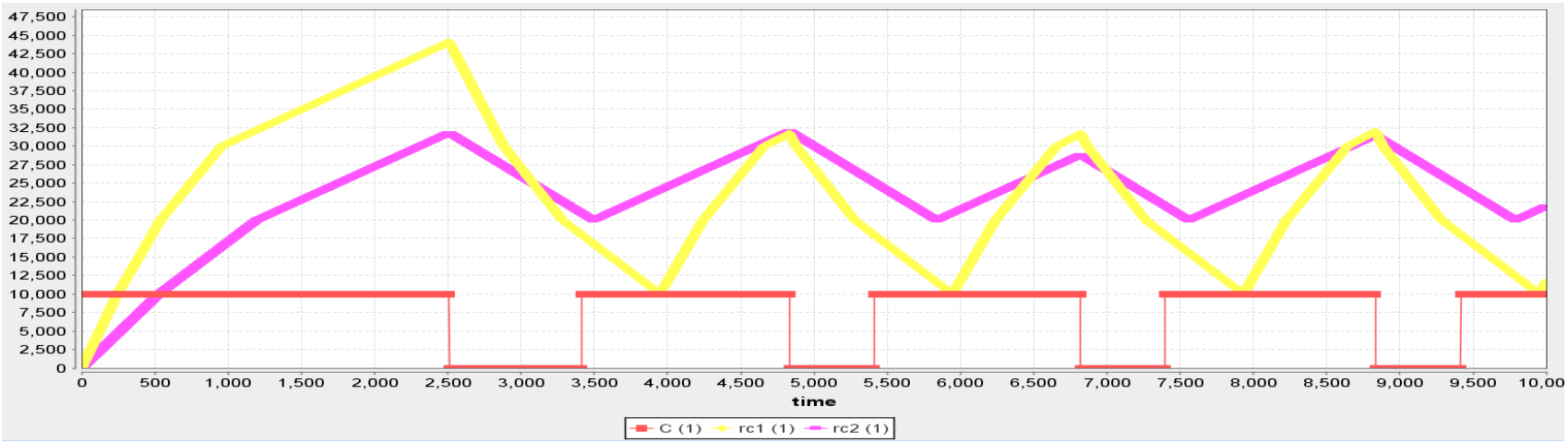


- Improved model

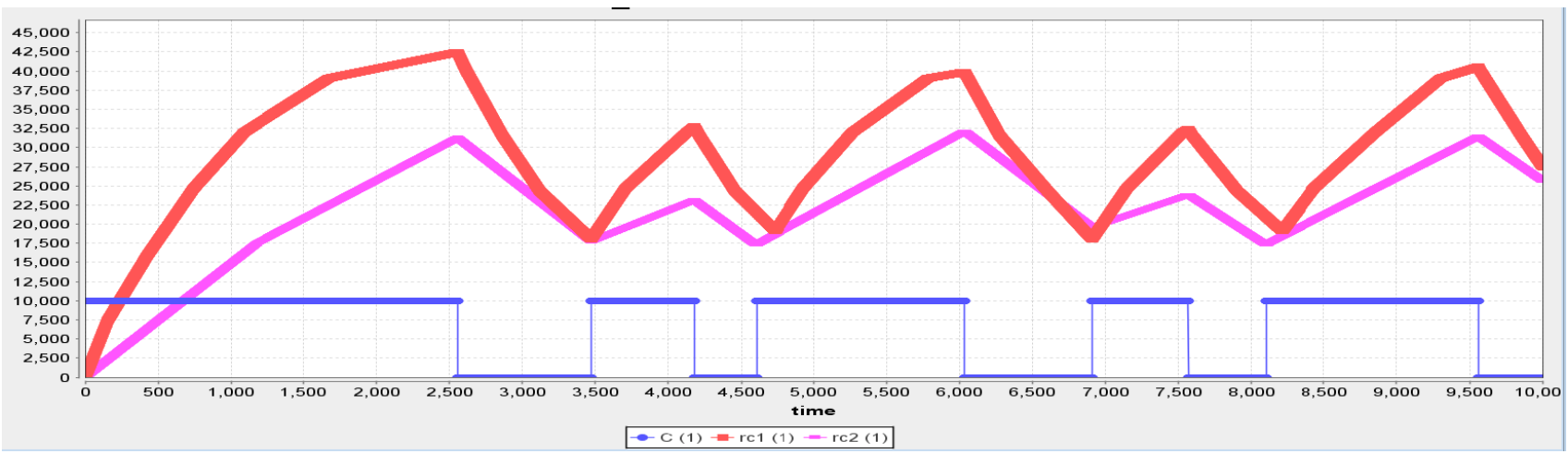


Or Element Model Simulation

- Original model



- Improved model



Conclusion and Future Work

- Our method provides an improvement to the existing method that provides a finer control over ranges of rates and the model structure.
- Future work:
  - Pseudo transitions,
  - Interpolation of data rules, and
  - Improved conflict resolution algorithm.