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Model-based design of asynchronous controllers for flexible on-chip power buffers

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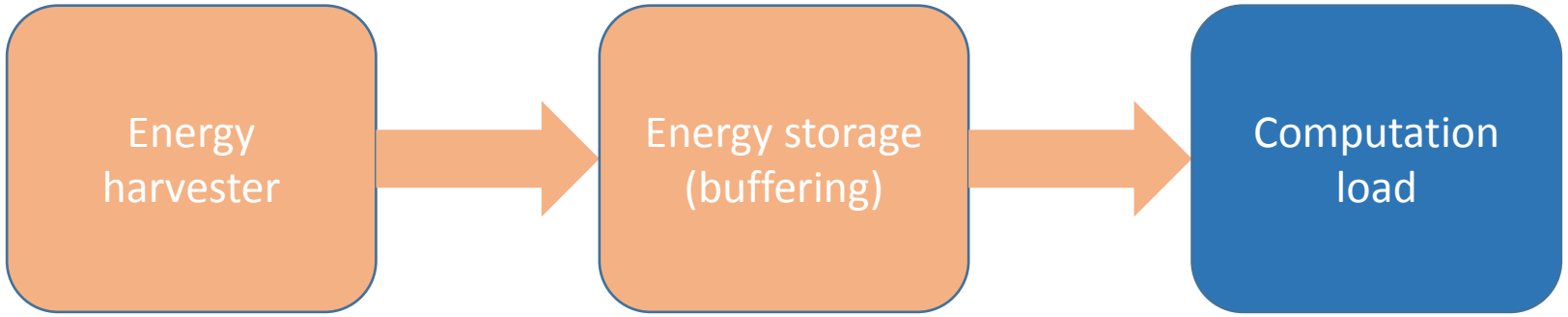
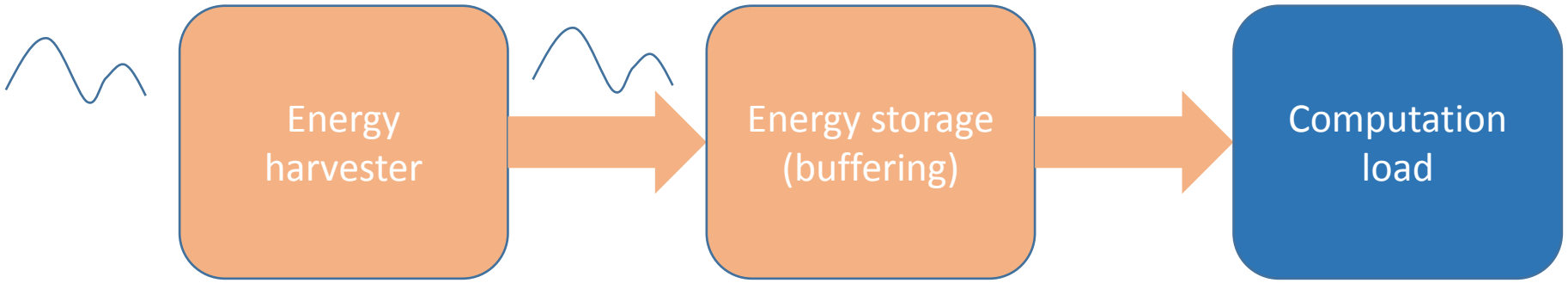
Energy buffering

- Energy buffering is important for systems based on energy harvesting



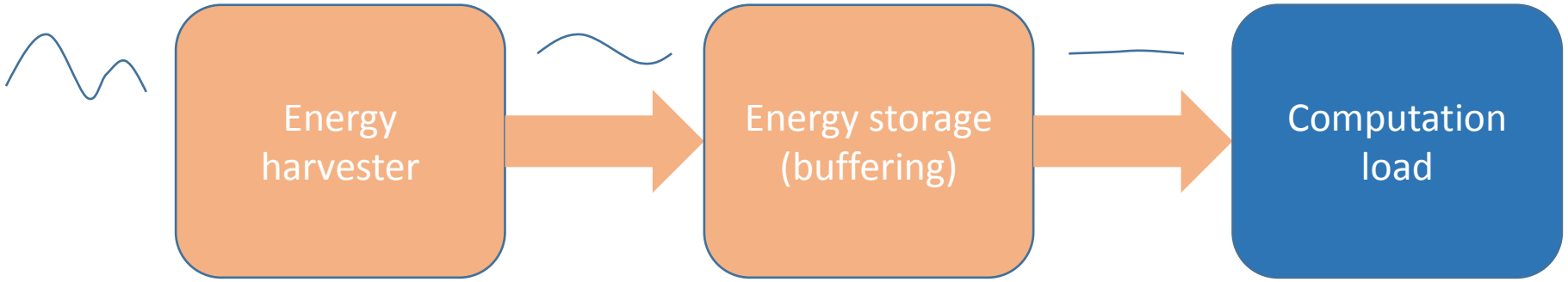
Energy heterogeneity

- Energy in the environment is variable
- Harvester output is therefore variable



Stable energy from unstable supply

- Conventional solutions emphasize delivering stable energy to load given uncertain energy in the environment ☺



☹ Costs include longer waiting time, broken supply, higher overheads, etc.

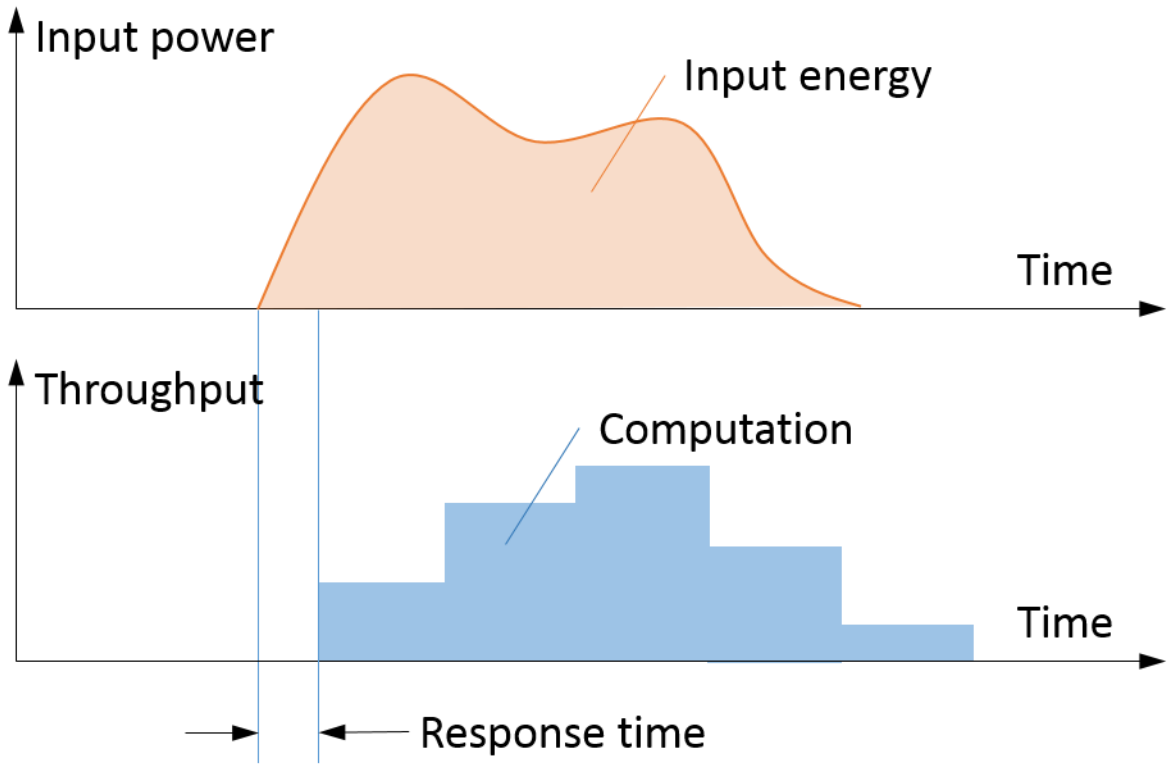
- Does the load actually want/need this level of pampering?

Load heterogeneity

- Computation loads may be highly heterogeneous
  - Asynchronous loads or loads which can be controlled by DVFS can work under a large range of voltage fluctuations
  - Different workloads may require different levels of energy
    - Small amounts of energy may be good enough to start harvester control and optimization computation to tune the harvester according to the environment
    - Small amounts of energy may be used to keep the computation alive
    - Flexible precision, compute/comms tradeoff, etc.

Energy and Load matching

- Trying to always provide stable Vdd with good power quality may not be necessary, or even desirable
  - Energy to task matching / energy modulated computing
  - Min response time
  - Max computation
- Paradigm: Energy is unlimited, but power is constrained and unstable



We are basically interested in:

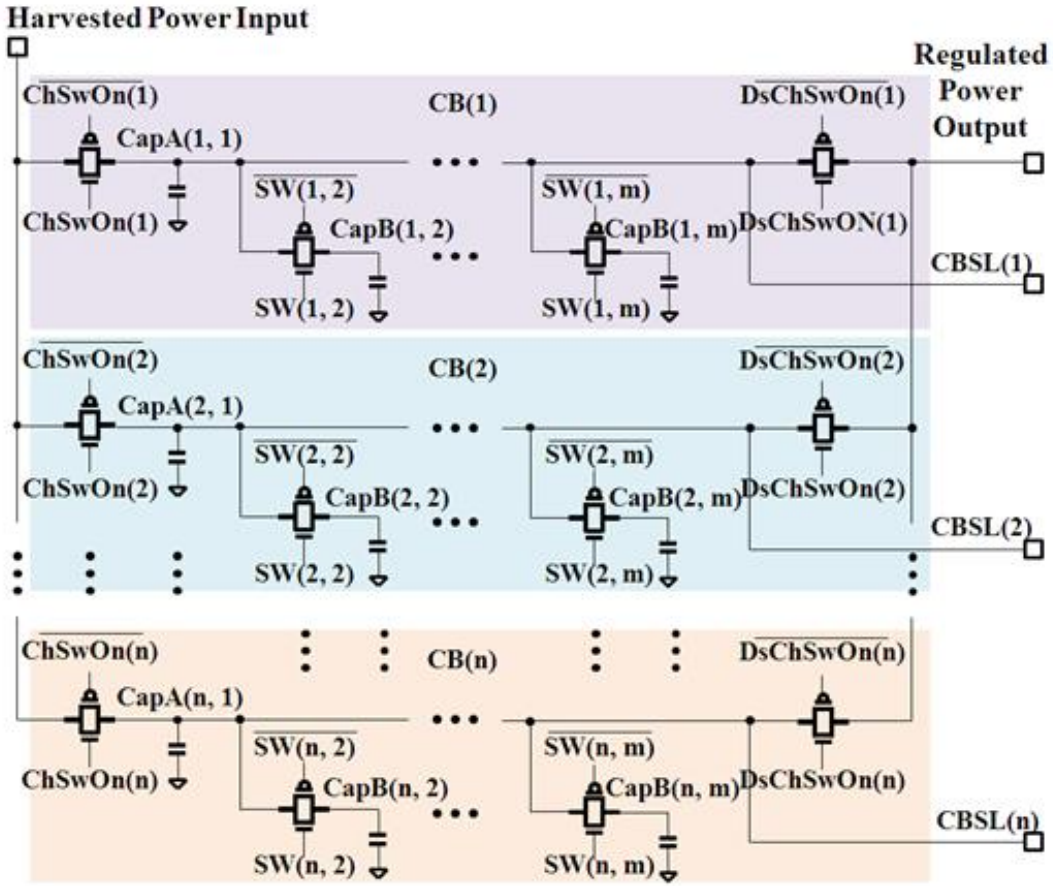
Power-compute co-design

Energy storage

- Off chip
  - Batteries
  - Supercaps
  - Inductive storage
  - Large capacity, potentially high efficiency
  - May be limiting factor for very small systems (overkill) and lack nimbleness for highly heterogeneous applications
- On chip
  - Switched capacitor converters (aiming to deliver constant/reliable Vdd)
  - Capacitor bank blocks (more general form supporting heterogeneous source/load matching)

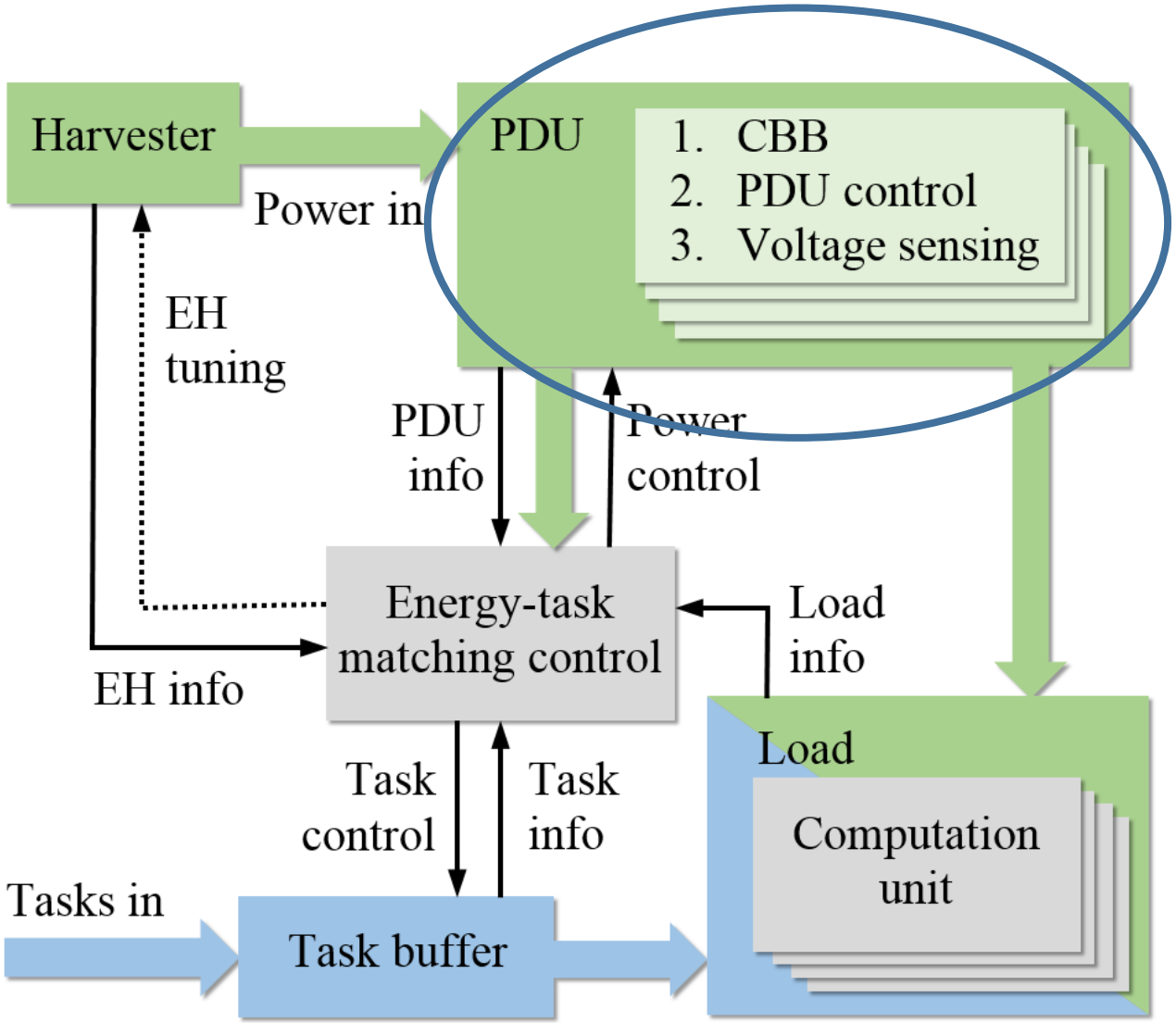
Capacitor Bank Blocks (CBB)

- CBB with capacitance adjustment facilities
  - Consists of a number of CB's
  - Each of which may contain a number of capacitors



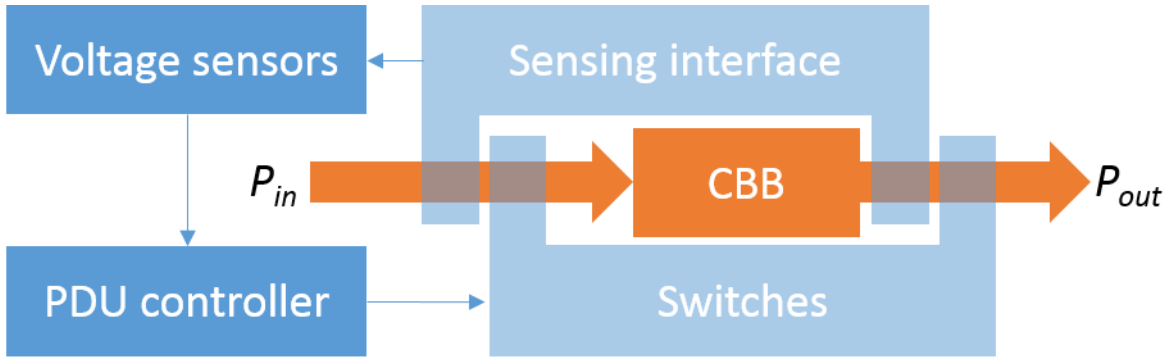
Energy source-load matching

- A system overview



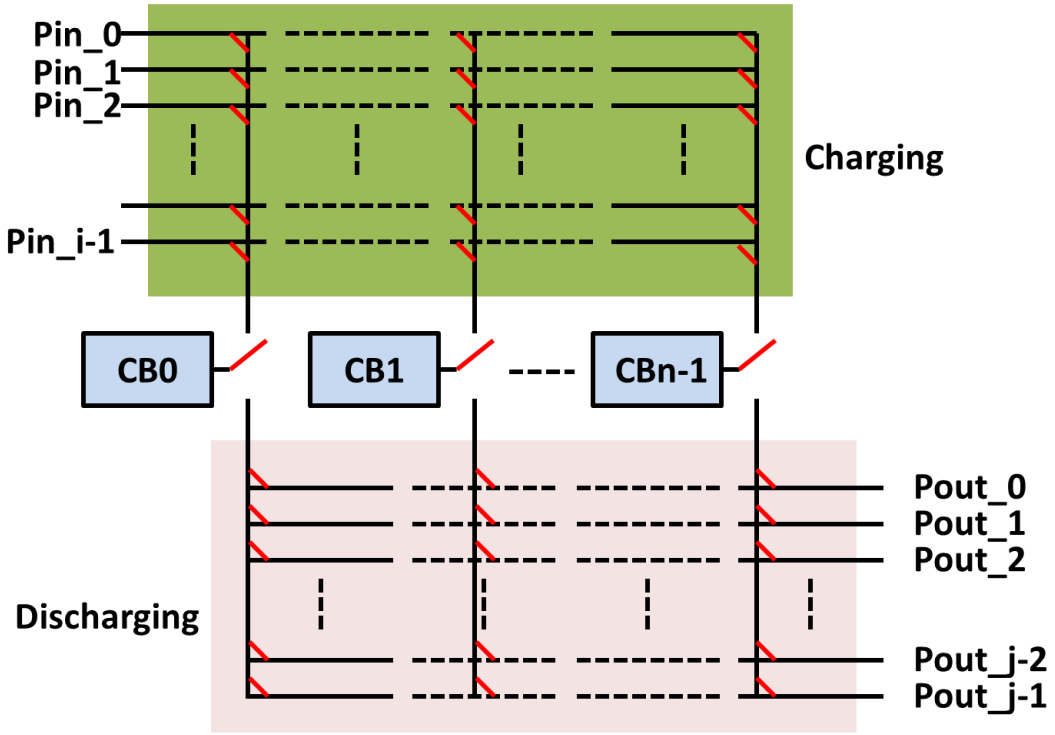
PDU overview

- CBB surrounded by sensing and switch interfaces
- Sensors monitor input, output and CB voltage values
- Switches implement charging and discharging connections
- Controller determines the charge and discharge actions based on monitored values and optimization algorithms



CBB charging and discharging switching

- Power in and power out (P_{in} and P_{out} wires) connected and disconnected according to charging and discharging decisions



From the CBB architecture

- Possible control decisions
  - Charging a particular CB up to a certain voltage from a particular P_{in}
  - Discharging a particular CB down to a certain voltage into a particular P_{out}
- Max energy management flexibility supported
  - Value of each CB can be tuned at design time to target potential source/load specifications
  - Full charge/discharge connectivity is supported for any **i** energy inputs and **j** energy outputs
  - Only hard assumption is that a CB is not charged and discharged at the same time – this is not usually a good idea
  - A CB can have a value of zero – direct connection from source to load

Maximum charge/discharge flexibility

- Max simultaneously charging CB's

$$\max_{CBB} N_{ch} = \min_{CBB}\{N_{CB}, N_{P_{in}}\}$$

- Max simultaneously discharging CB's

$$\max_{CBB} N_{dsch} = \min_{CBB}\{N_{CB}, N_{P_{out}}\}$$

- Max simultaneously charging and discharging CB's

$$\max_{CBB}\{N_{ch} + N_{dsch}\} = \min_{CBB}\{N_{CB}, (N_{P_{in}} + N_{P_{out}})\}$$

Without losing generality

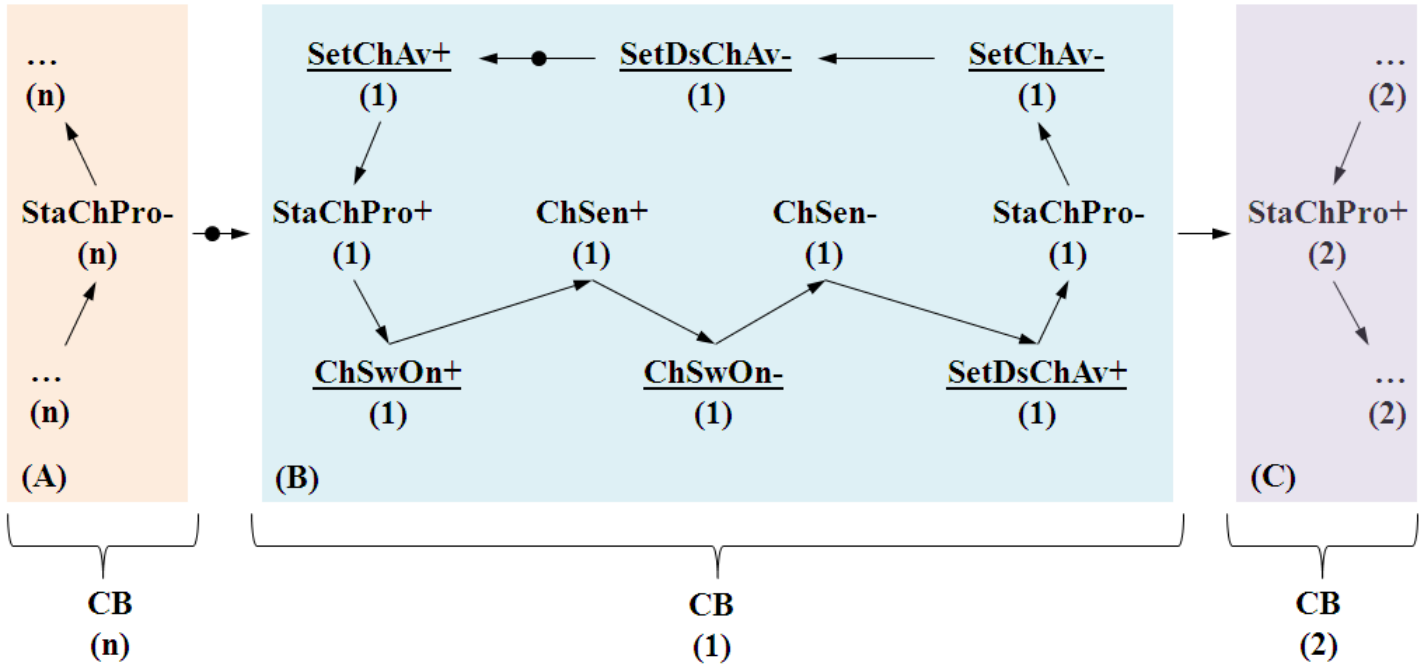
- Let's look at PDU design for a single EH / single load case

$$N_{P_{in}} = N_{P_{out}} = \max_{CBB} N_{ch} = \max_{CBB} N_{dsch} = 1$$

- A CBB with multiple CB's can be connected to the single power in and single power out in a number of ways
  - Full random charging/discharging access – like RAM
  - Cyclic access (first in first out) – like FIFO
  - Other access rules with similarities to data memories can be implemented
- In this work we demonstrate asynchronous PDU controller design through a FIFO CBB control example
  - Asynchronous controller for event-driven, low overhead functionality

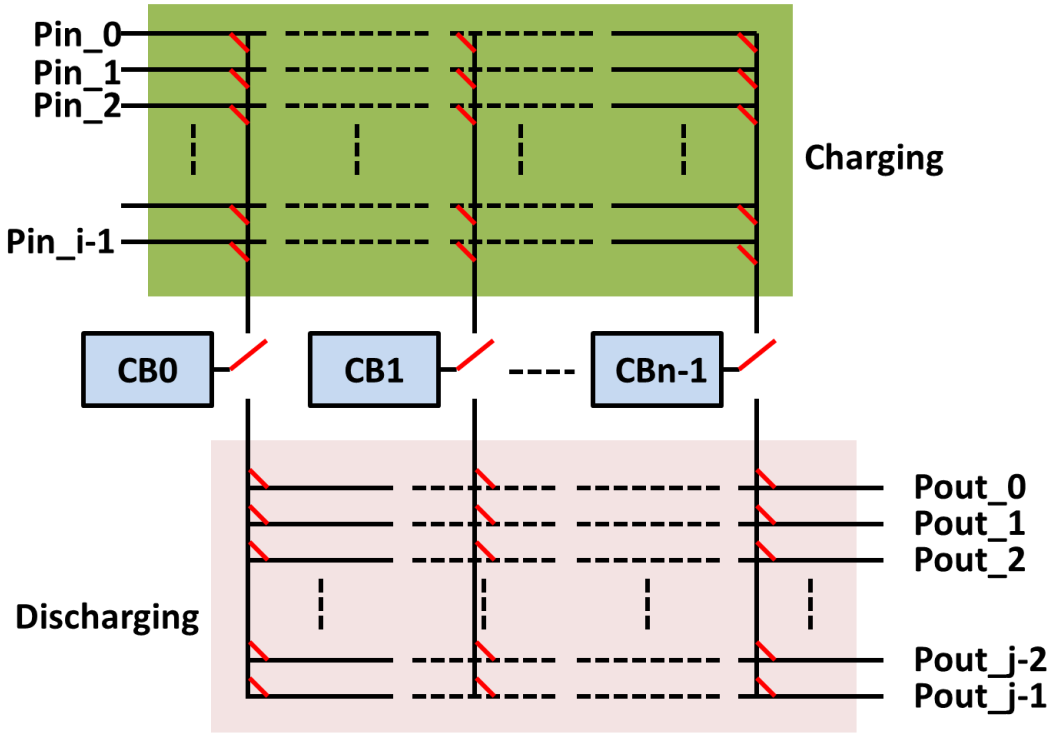
Charging control

- Charging is done in a FIFO cyclic manner
- Only when the current CB is charged up to the prescribed voltage is the next one ready
- When charging chases up discharging, the switch at the CB decides if the CB should be in charging or discharging



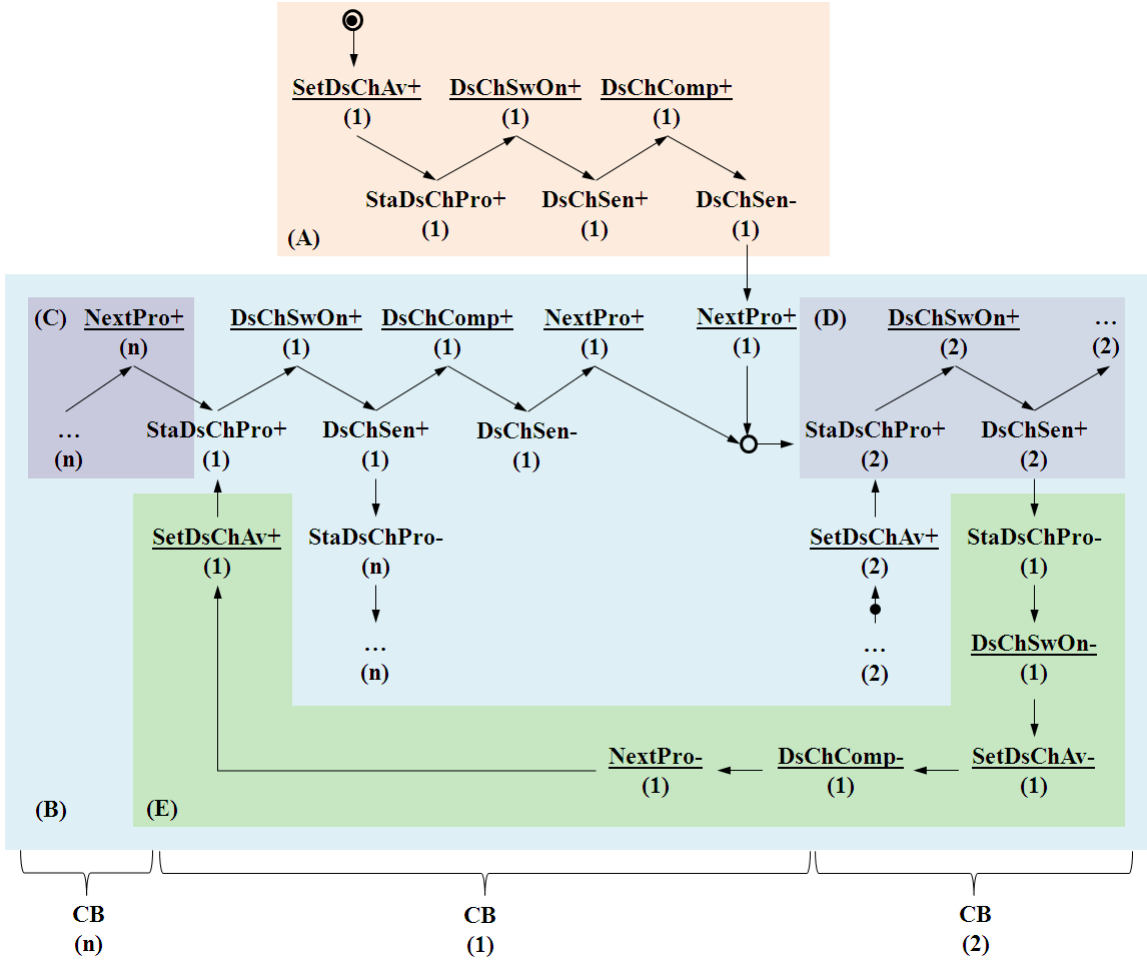
CBB switch network review

- Note the switches at the CB's – either up or down but not both



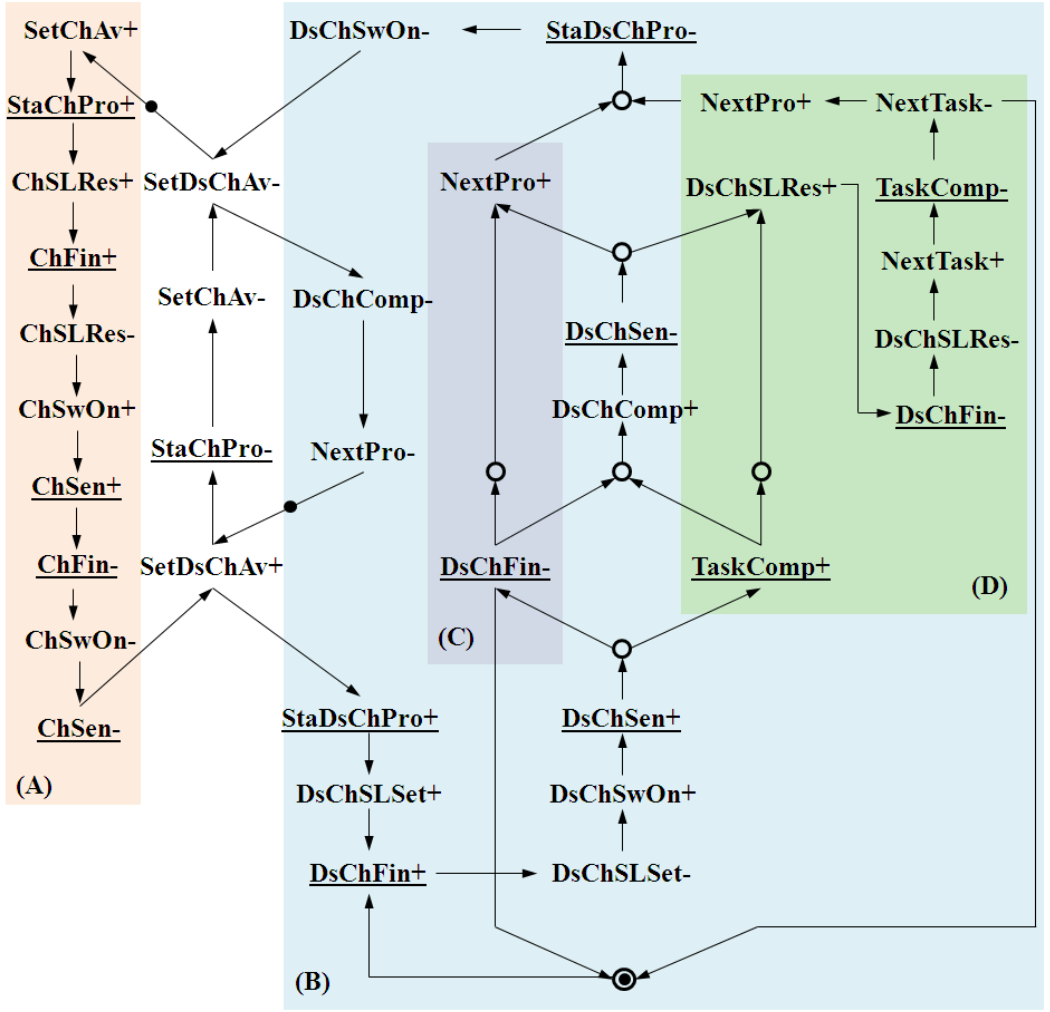
Discharging control

- Discharging is also FIFO cyclic
- (E) ensures continuous power if the CBB is not depleted entirely
  - Discharging on CB_1 stops only after CB_2 has already started discharging (overlap)
- (A) assumes global initialization with no energy in the CBB
- (B) main discharging control
- (C) neighbouring CB's



Charging and discharging for each CB

- (A) charging cycle
- (B) discharging cycle
- (C) when low end of discharging range is reached (end discharging of this CB at target voltage)
- (D) when the task is completed (end discharging when load finishes execution – not a control action based on CBB sensor readouts)



Experimental results

- Entire design of the CBB block validated including
  - CB's
  - Sensors
  - Async CBB FIFO controller
  - In UMC 95nm CMOS
- Controller overheads negligible
  - Energy delivering efficiency mostly depends on correct source-load matching
  - Control algorithm needs to balance charging efficiency with discharging efficiency to optimize overall energy delivery efficiency

Non-FIFO designs

- Concurrency in charging and discharging is already possible with the FIFO design
  - Different CB's can be charged and discharged at the same time
- Other access rules can be implemented using the STG method
  - The per-CB access control is entirely general and without any inter-CB dependency
  - This allows a CB to be charged and discharged (not simultaneously) without regard to previous charging and discharging history of itself and other CB's, so long as the charging and discharging ranges are realistic
  - You cannot prescribe charging a CB to a voltage lower than its current voltage, or discharging a CB to a voltage higher than its current voltage

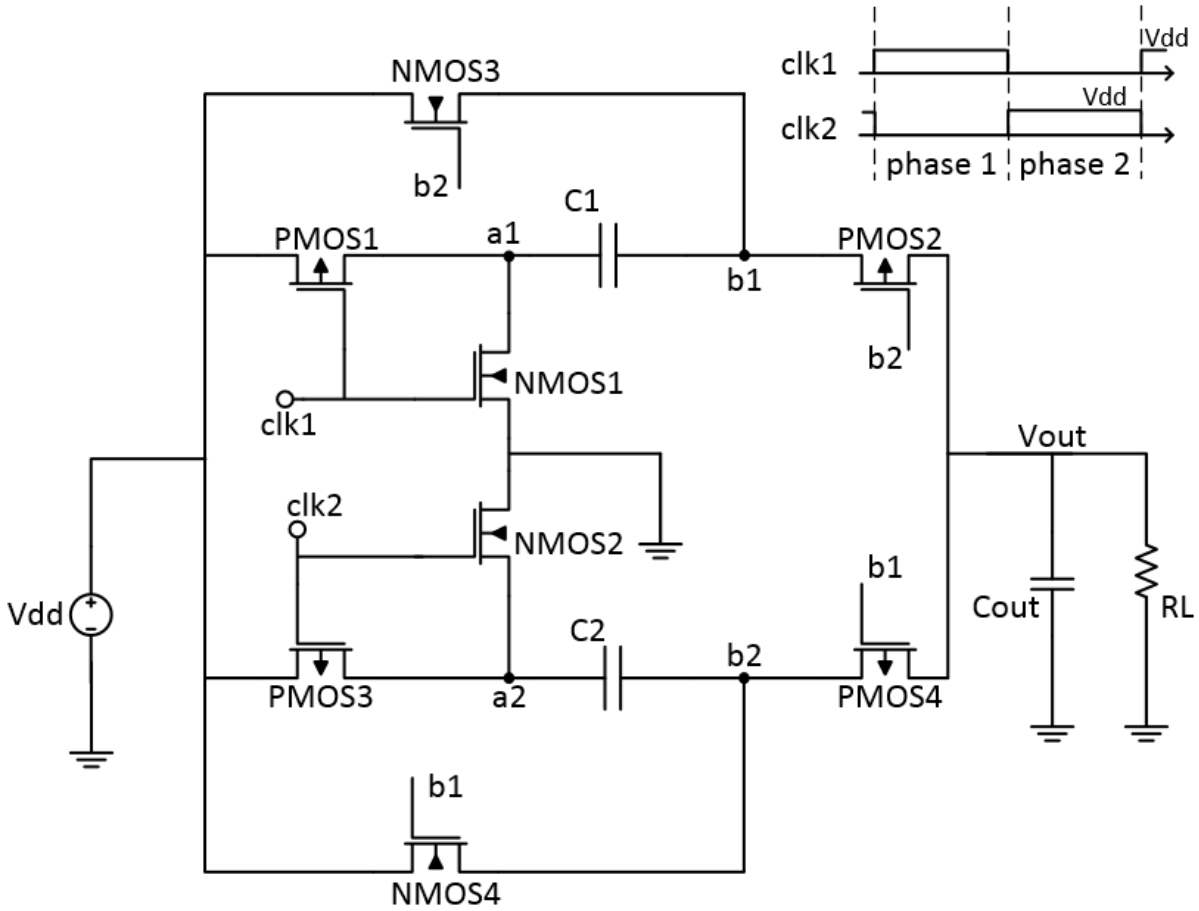
Take-home message

- CBB supports on-chip energy buffering with fully flexible energy flow control
  - From high output power quality to high output power heterogeneity
- The general CBB structure and single CB control knobs provide highly flexible access control options
- Asynchronous controller is best suited for CBB buffers offering naturally event-based operations to higher level energy-load matching management
  - Ease of design with STG's
  - Low overhead implementations

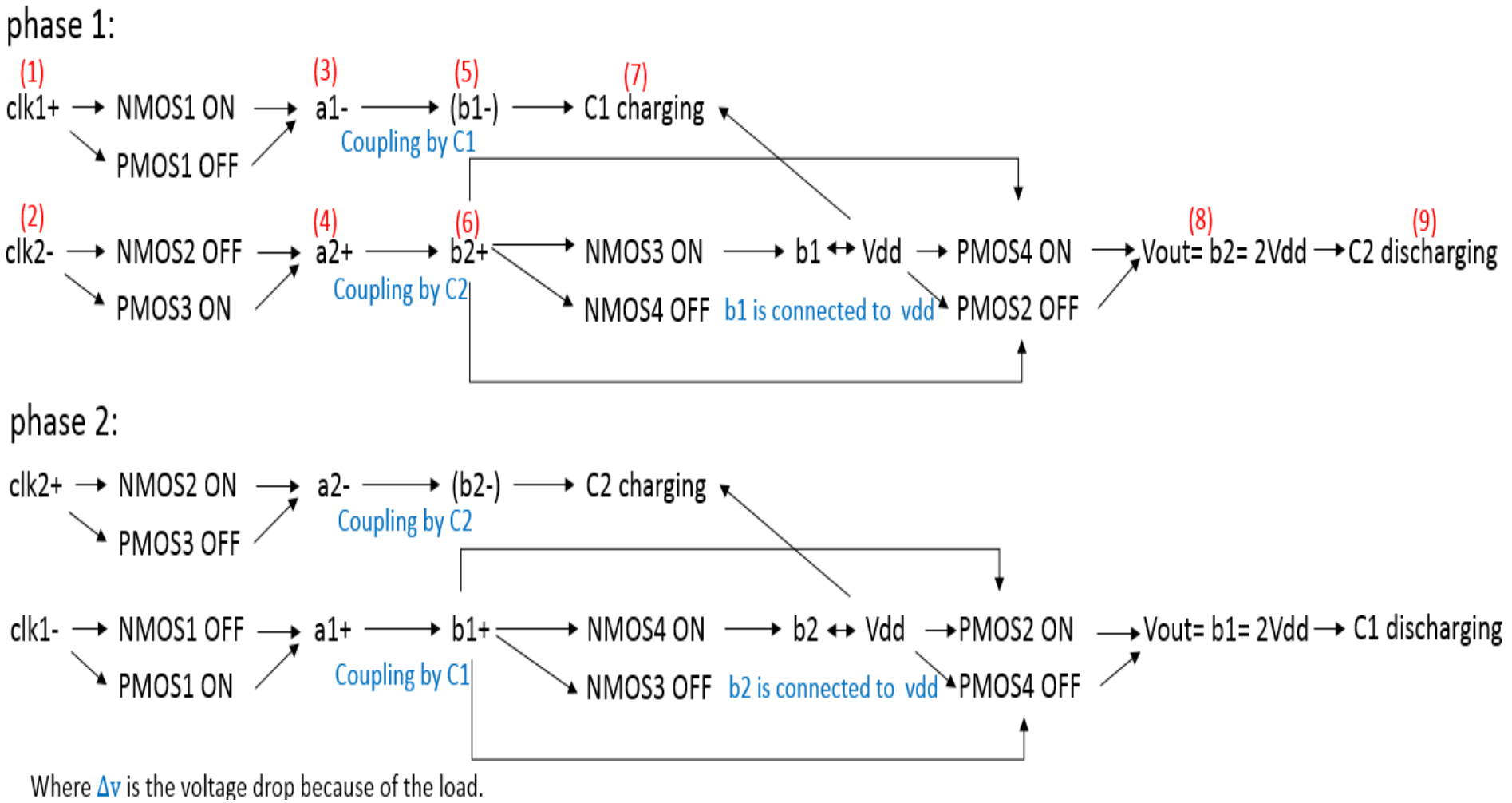
On-going and future work

- Developing STG models for mixed-signal switching capacitor circuits
- Include ways to represent causality based on logic signal transitions and capacitive coupling
- Application to DC-DC converters, e.g. optimal charge sharing for bottom plate parasitic caps
- Analysis will include verification and synthesis of controllers
- Automation will include incorporation into Workcraft

Example: voltage doubler



Voltage doubler: STG



Thanks