Speeding up Repeated Analog Simulations for Reliability and Testing

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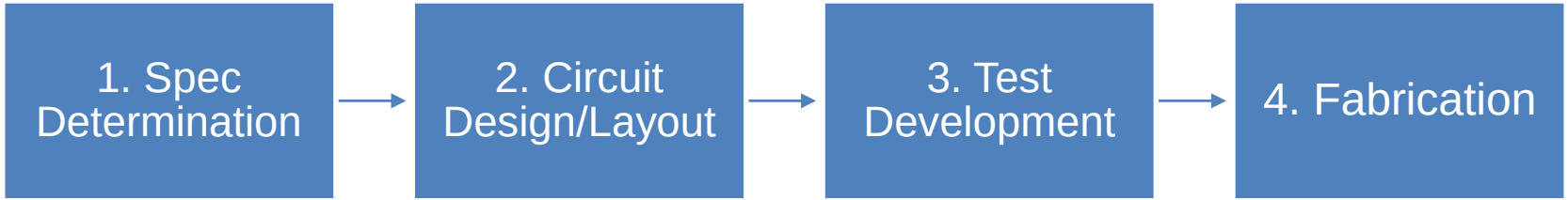
Introduction

- Integrated Circuits increasingly used
  - Vehicles: > 400 ICs
- Testing necessary: safety-critical applications
  - (Autonomous) Vehicles
  - Biomedical applications

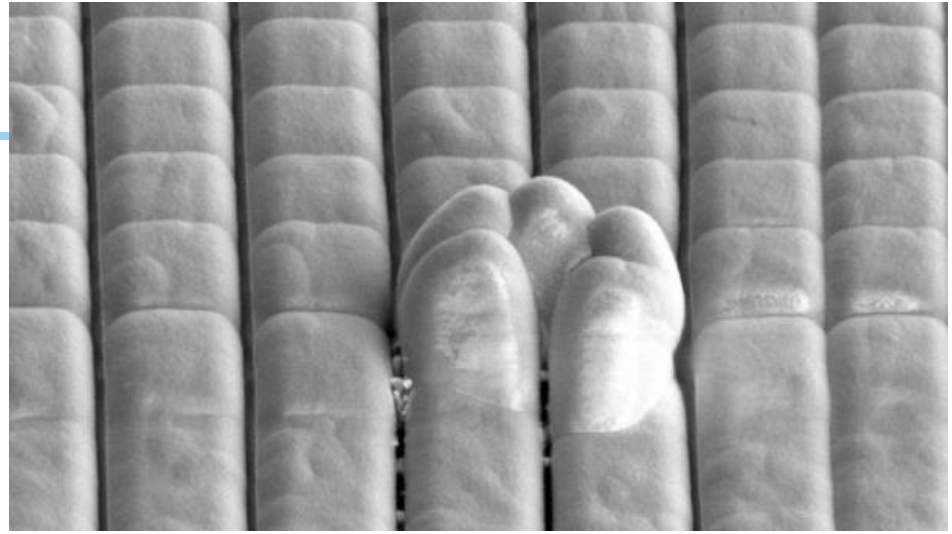
Alnalog IC design flow



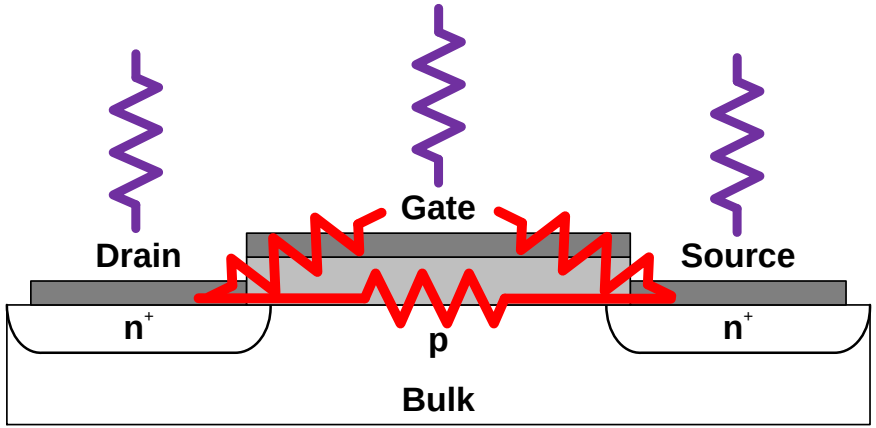
- Design/layout account for fabrication variability
  - Parametric focused
- Manual processes

Defects & faults

- Catastrophic defects
  - Random
  - Assume one at a time

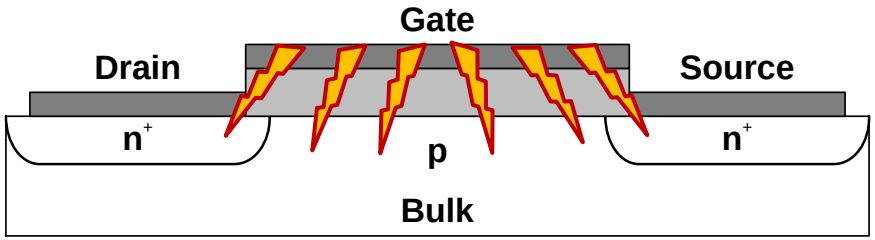


- CMOS (& BJT)
  - 6 fault resistive model
  - Short (low ohmic)
  - Open (high ohmic)



Latent defects & faults

- CMOS
  - Gate oxide example
  - Time-dependent dielectric breakdown of gate oxide
- Activation condition
  - Latent → catastrophic



$$\tau_{BD} = \tau_0(T) \cdot \exp\left(\frac{G(T) \cdot t_{ox,effective}}{V_{ox}}\right)$$

$$V_{stress} \geq \frac{\ln(\tau_{life}) - \ln(\tau_0)}{\ln(\tau_{test}) - \ln(\tau_0)} \cdot V_{nom}$$

Outline

- Fault simulation methodology
- Automatic test generation
- Simulation speed-up & automation

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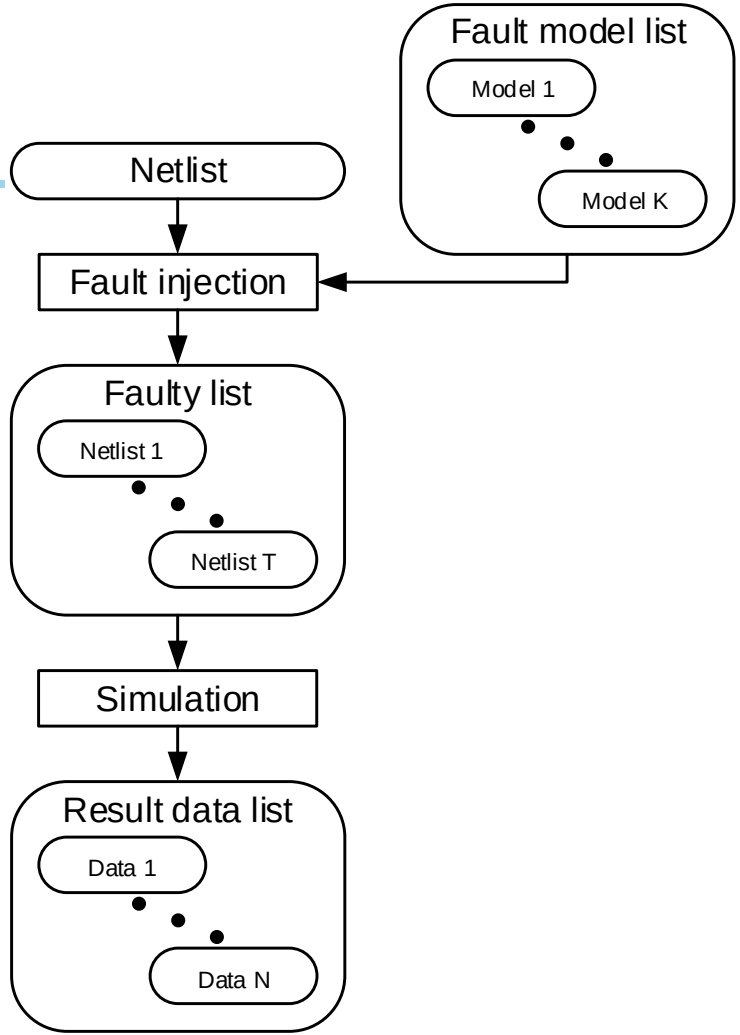
Fault simulation flow

- Circuit description
- Fault injection
  - Inputs: fault model, netlist
- Netlists simulation
- Result analysis



Defect-oriented tests

- Fault coverage $FC = \frac{\sum Detected\ faults}{\sum Faults}$
  - Good Circuits (Monte Carlo) ←→ Faulty measurement
  - Area weighted coverage $FC_A = \frac{\sum_i D_i * A_i}{\sum_i A_i}$
- Fault Activation Coverage FAC
  - Latent defects
- ~Optimization metric

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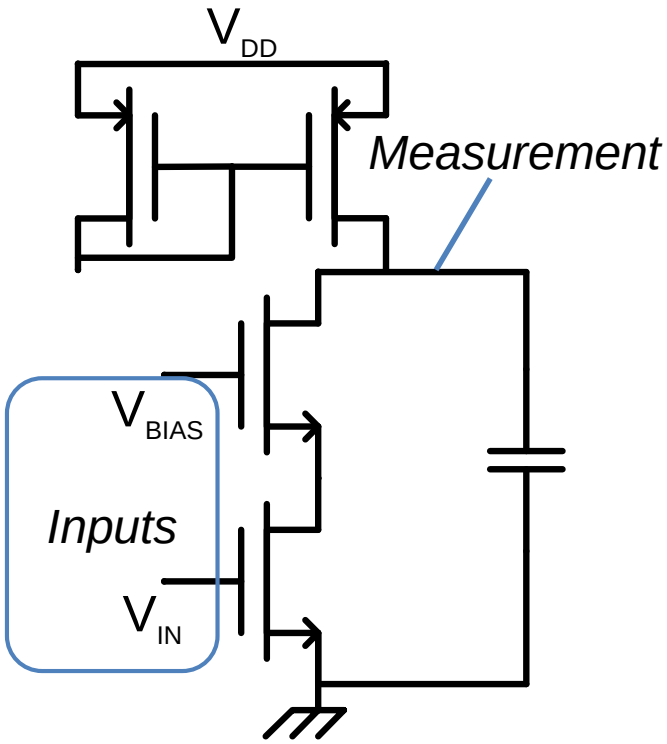
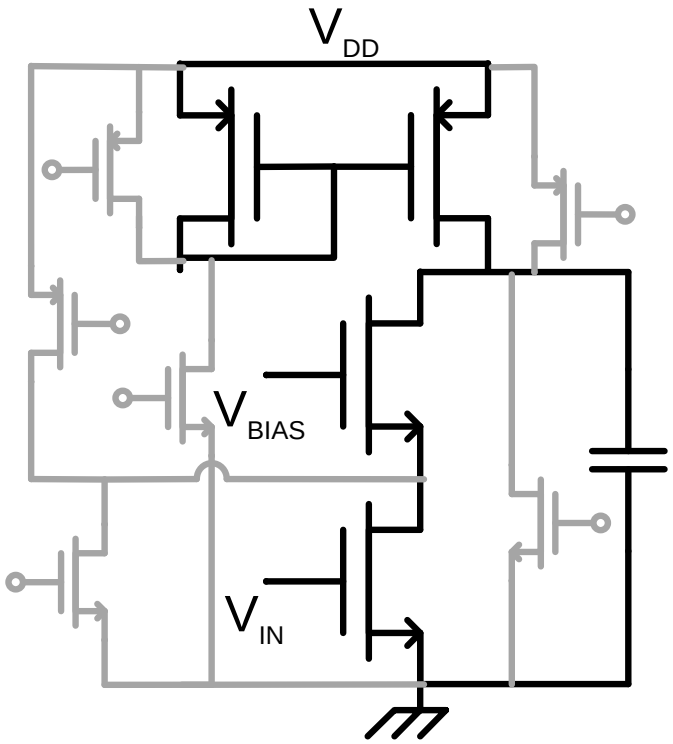
Test generation

- ATSG
  - $\max FC(V_{bias}, V_{IN})$
  - Using some measurement
    - Current consumption
    - Voltage probe
- Optimization
  - Differentiable?
  - Existence of local maxima?
  - Genetic optimizer



Test generation

- Design-for-Test
  - Ex. Topology Modification
  - Pull-up/pull-down modes
  - Other structures possible
- Tests selection
  - $\max FC(Topology_i)$
  - Discrete optimization



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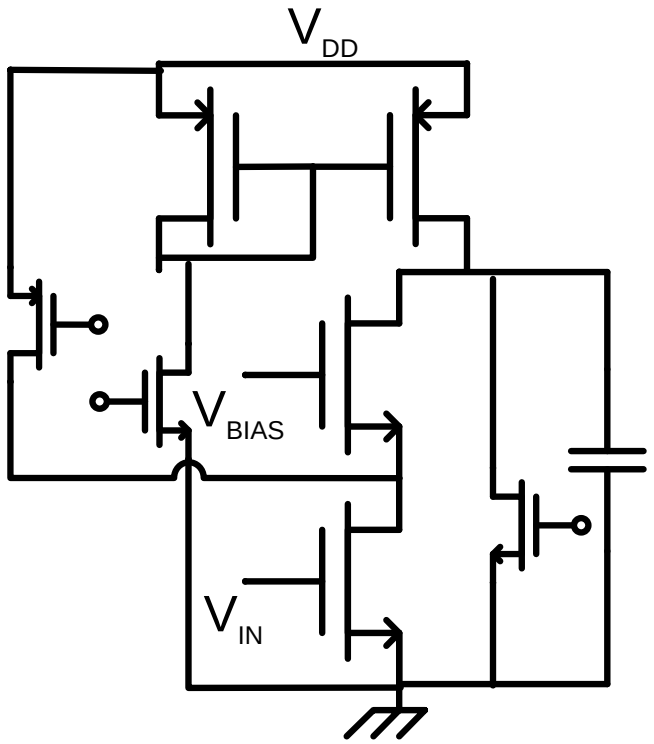

Scalability issues

- Netlists simulation (DC)

  $\sim \underbrace{\alpha}_{\text{Solution precision}} * \underbrace{nodes^3 * devices}_{\text{Circuit size}} * \underbrace{faults/device}_{\text{Fault models}}$

- ATPG: unknown number of evaluations
- TM: ** 2 * nodes*
  - Possible for smaller circuits using multi-objective Genetic Optimizer

Other issues

- Can the impact of adding DfT be fully assessed?
  - Designers tend to not like adding test structures…
- ATSG to generate activation condition
  - Same issues as ATSG, but with internal node

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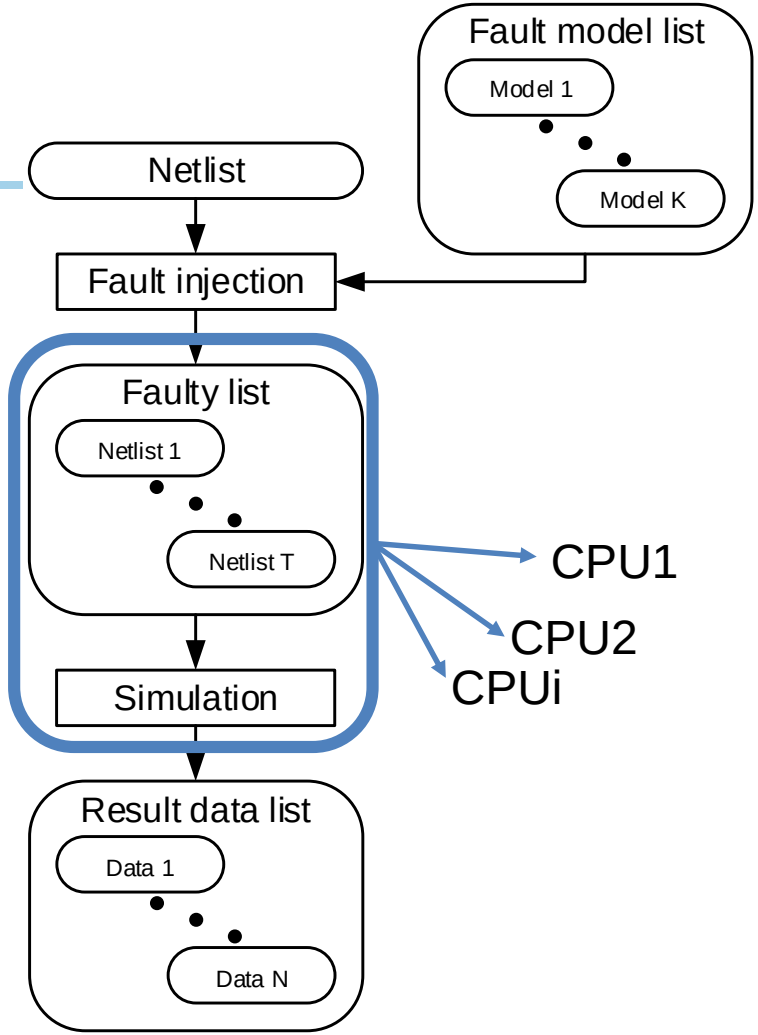
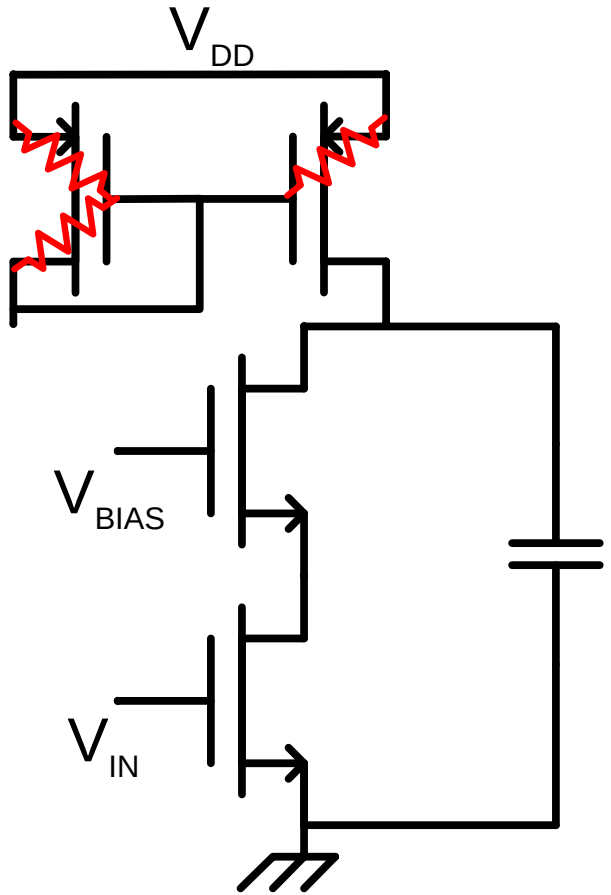
Speed optimizations

- Parallelization of Simulations
  - Faulty circuits independent from each other



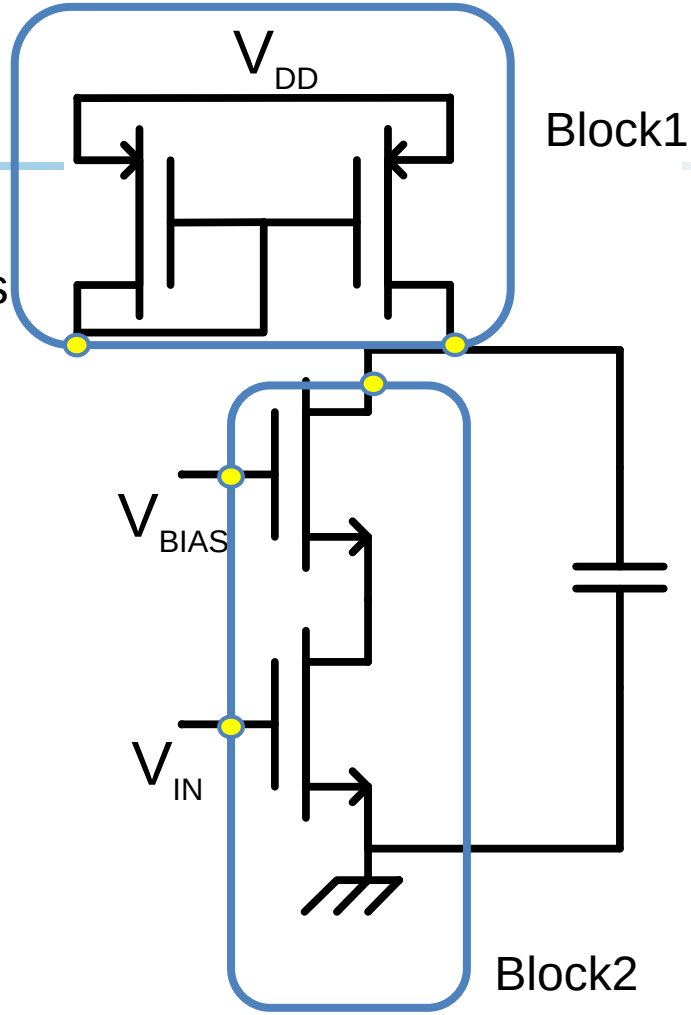
Speed optimizations

- Fault contraction
  - Transistors with common node connection have similar faults
  - Diode-connected transistors
- Remove duplicate faults
- Only applicable to shorts



Speed optimizations

- Split circuit in blocks
  - Block boundaries defines by nodes
  - Division decided by Simulated annealing
- Built piece-wise linear model of each block (good & faulty)
  - $i_1 = f(v_1, v_2, \dots)$
- ATSG:
  - ‘Invertible’ model of each block
  - Signal propagation to measurements
  - Interval analysis: detection range
  - If not detected: add DfT



Speed optimizations

- ~ α * *accuracy* * *Blocks* * *nodes*^{3} * *devices* * *faults/device*
- PWL ‘inversion’ possible
- Memory use
- Significantly less DfT

Implementations

- Topology Modification
  - 35-transistor voltage regulator
  - >90% fault coverage
  - >76% fault activation coverage
- ATSG + TM
  - 50-transistor analog multiplexer
  - >98% fault coverage
  - Blocks have 3 terminals max

Conclusions so far

- Methods aimed to be generic
- PWL models allow ATSG for larger circuits
  - ~GBs memory
  - ~hours computation time
- Good results for smaller circuits

Further work

- Higher order piece-wise functions possible?
  - Spline approximations?
  - ‘Inversion’ possible?
  - Trade-off CPU-time vs. memory?
- Other methods for block division?
  - Optimal number of terminals?
- Transient simulations?

References

- A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, “Automated testing of mixed-signal integrated circuits by topology modification,” in *VLSI Test Symposium (VTS)*, 2015
- A. Coyette, B. Esen, W. Dobbelaere, R. Vanhooren, and G. Gielen, “Automatic test signal generation for mixed-signal integrated circuits using circuit partitioning and interval analysis,” in *2016 IEEE International Test Conference (ITC)*, 2016
- N. Xama, A. Coyette, B. Esen, W. Dobbelaere, R. Vanhooren, and G. Gielen, “Automatic testing of analog ICs for latent defects using topology modification,” in *European Test Symposium (ETS)*, 2017
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