Trends and Challenges in Analog and Mixed-Signal-Verification

Dieter Haerle
17.5.2018

Agenda

1. Introduction Presenter
2. Definitions
3. Motivation
4. What is „Analog-Mixed-Signal Verification“?
5. History / State of the Art
6. Trends and Challenges in AMS-Verification
7. Conclusion

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Dieter Haerle

- Dieter Haerle, KAI (Kompenzzentrum für Automobil- und Industrieelektronik) Research institute owned by Infineon Austria
- Project Manager for research projects
- Steps in my career
  - 1990-1996 Studies of Electrical Engineering at TU Karlsruhe, Germany
  - 1996-1999 R&D department of semiconductor memories at Siemens, Munich
    - analog design
  - 1999-2003 Semiconductor Division of Mosaid Technologies Inc, Ottawa, Canada
    - analog design, concept engineering, technical design team lead
  - 2004-2014 Automotive Division of Infineon Technologies AG Austria, Villach
    - analog design, concept engineering, line manager, technical design team lead
  - 2014 –present Kompetenzzentrum für Automobil- und Industrieelektronik GmbH
    - project manager
- Personal
  - Family, 2 children
  - Scuba Dive Instructor, ballroom dancing, Salsa, snow boarding, cycling, cooking

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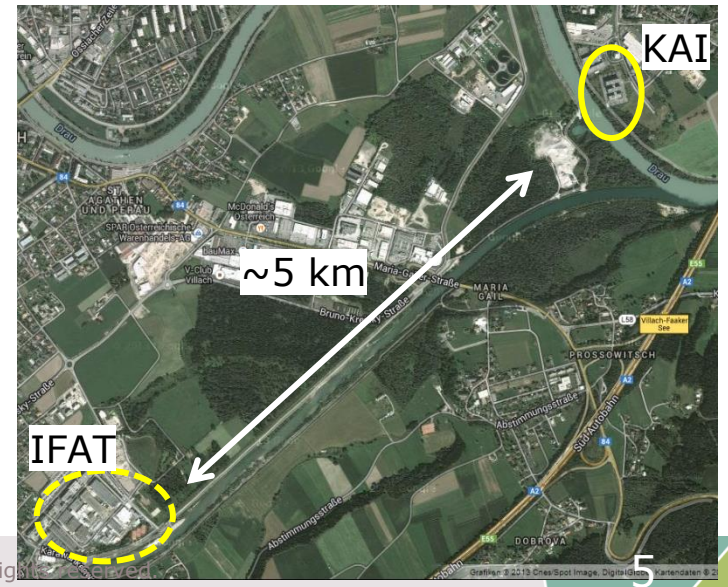
KAI – competence center

- **K**ompetenzzentrum **A**utomobil- und **I**ndustrielektronik GmbH (www.k-ai.at)
- Scientific work on **predevelopment** topics in the course of **applied research** in close cooperation with the Infineon development engineers
- Fostering of the **scientific network** through cooperation with **universities** and attendance of conferences
- Active **cross business unit** knowhow transfer
- **Education** of future IFAT **employees**



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KAI - Facts & Figures

- Foundation : 12/2005 as a cooperative research center
  - Since Oct. 2013 a 100% subsidiary of IFAT (Infineon Technologies Austria AG)
- Office / Laboratory in total ca. 800 m² at Technology Park Villach
- Managing Director : Dipl. Ing. Josef Fugger, Mag. Peter Zeiner
- Employees: ~50
  - Thereof ~15 PhD students, ~5 MSc students,
    - ~10 more PhD students employed at university partners
- Financing: projects financed by Infineon and public funding
  - Funding project „EM2APS" in cooperation with Infineon Technologies and academic partners (FFG-Basisprogramm)
  - Active participation in European funding projects (Powerbase, SemI40)
  - Funding bodies: FFG, (KWF), ENIAC/ECSEL

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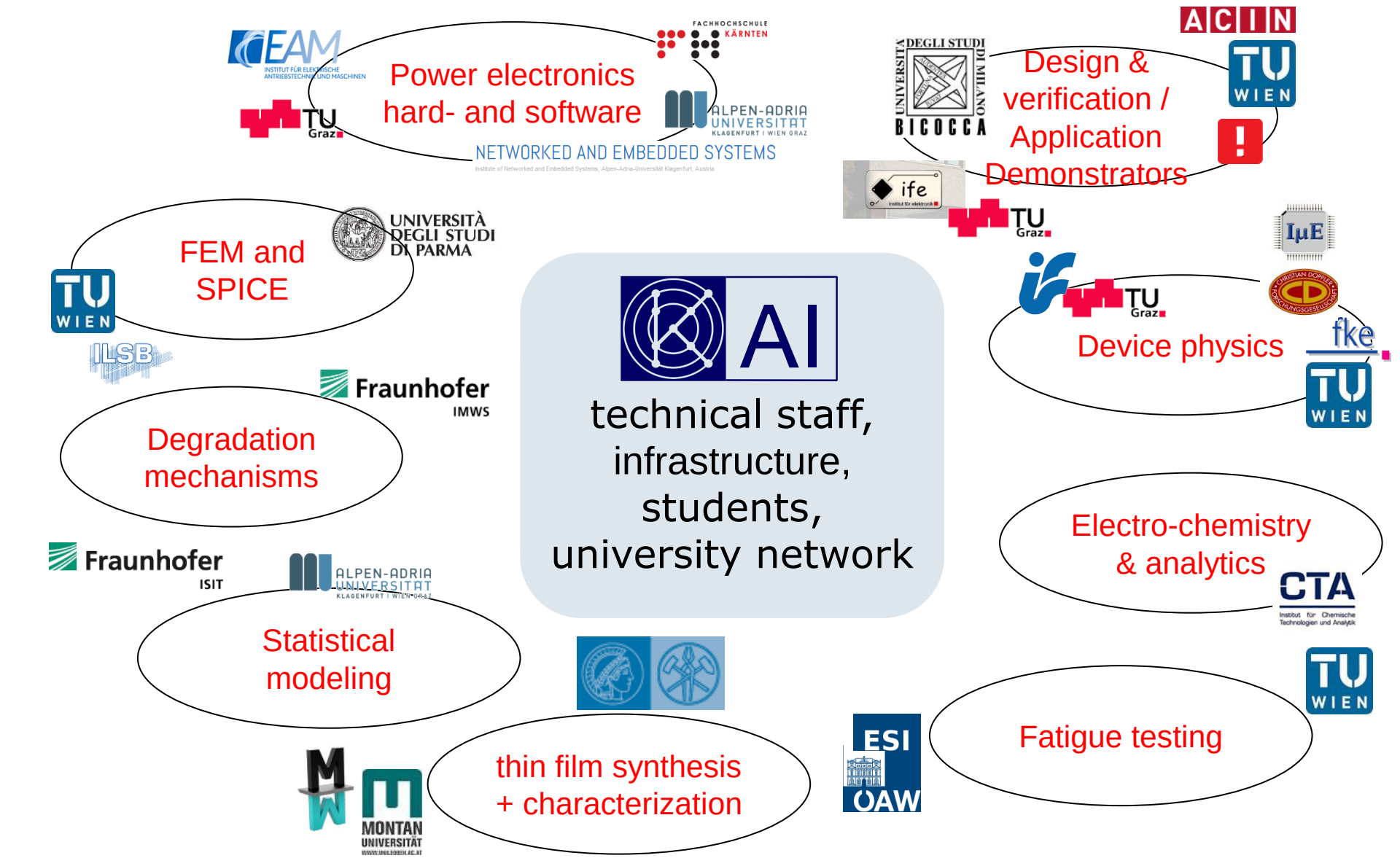
Research landscape KAI



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Definitions

- **Analog-Mixed-Signal design vs. Analog design** -> in this presentation mainly Analog-Mixed-Signal design is considered, because in my personal opinion pure analog design/verification is dying out and will only be used in very special cases anymore.
- The PMBOK guide (A Guide to the Project Management Body of Knowledge), a standard adopted by IEEE, defines Validation and Verification as follows in its 4th edition:
  - "**Validation**. The assurance that a product, service, or system meets the needs of the customer and other identified stakeholders. It often involves acceptance and suitability with external customers. Contrast with verification."
  - "**Verification**. The evaluation of whether or not a product, service, or system complies with a regulation, requirement, specification, or imposed condition. It is often an internal process. Contrast with validation."

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Verification is the science (and art) of asking the question, “What could possibly go wrong?” [Bryon Moyer]

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Motivation

- Increasing quality requirements,
- Increasing circuit complexity,
- Demand for faster development cycles,
- Increasing demand for traceability of requirements / specification points

currently drive the mixed signal verification methodology to its limits.

Situation:

- Simulation times are becoming excessively long
- Simulation complexity increases beyond the ability to cope with it.

New verification concepts have to be developed!

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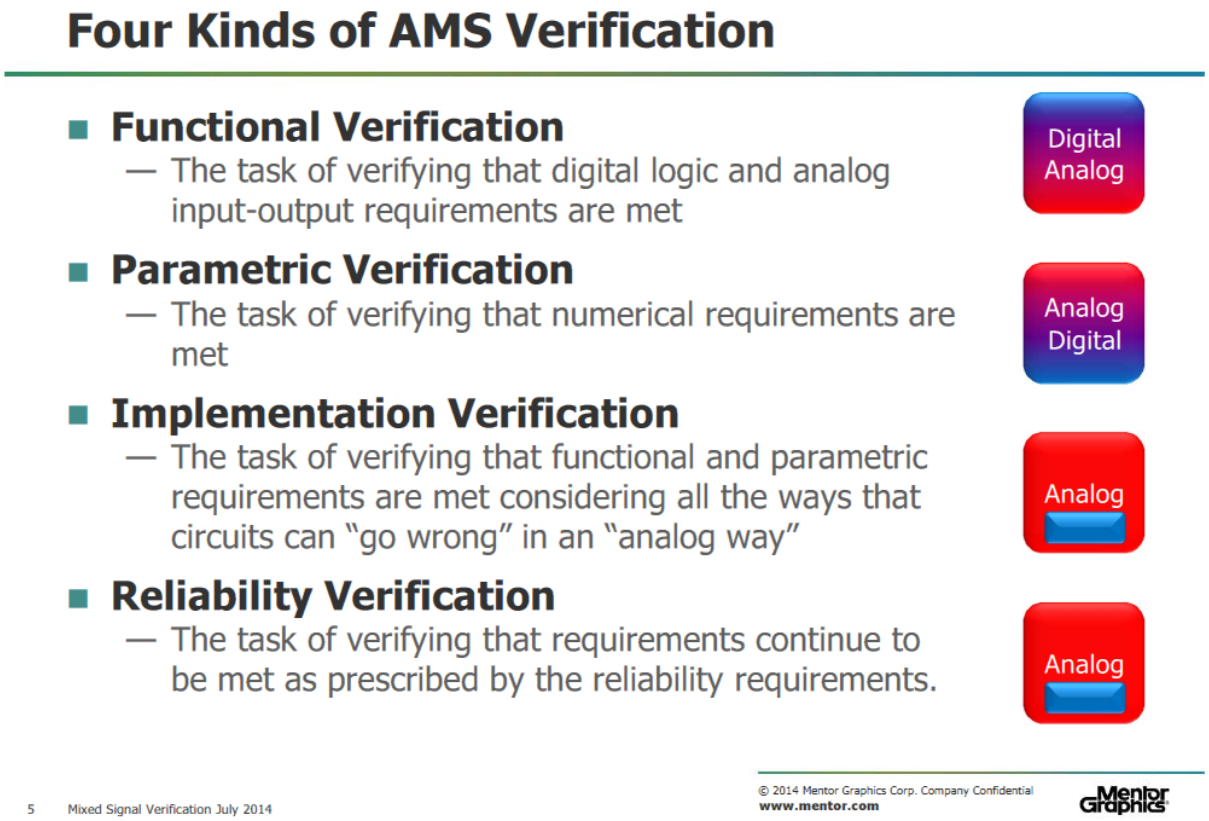
Understanding of Mixed Signal Verification 2011

Martin Vlach, Chief Technologist AMS, FAC 2014



Is this still true?

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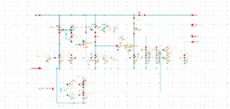
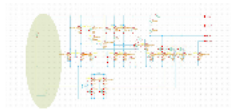
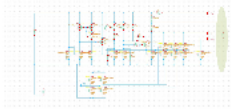
Analog Verification at the Beginning







- Rough customer specification
- Create circuit schematic
- Think about, what has to be verified first (first verification requirement)
- Create test bench in the same schematic and run one test to simulate/verify first verification requirement for nominal process parameters
- Think about, what has to be verified next (second verification requirement)
- Modify schematic with first test bench to be able to simulate/verify second verification requirement
- …

I have recently seen analog designers still doing it this way!!!!!

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Next steps done so far (not necessarily in this order)

- Separation of test bench and circuit schematic
- Introduce circuit abstraction in verification (modelling, …)
- Verification plan (including functional and parametric verification) before starting a verification
- Extending functional and parametric verification to EMC, ESD, … verification
- More precise specification for verification including verification conditions for specification parameters
- Moving to Analog-Mixed-Signal verification (analog and digital circuits together). Usually digital circuits are only used to stimulate the analog part.
- Separating design and verification tasks between design engineer and dedicated, specialized verification engineer
- Automated regression tests
- Analog/mixed signal UVM
- …

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Current Situation

- Extremely heterogeneous landscape regarding mixed signal verification (from pure single analog simulation done by the design engineer to extremely complex regression suites done by dedicated mixed signal verification specialists)
- Specification for analog circuits still done with unformal verbal text (prose text). Traceability of specification requirements very difficult.
- In many cases no reference model available for verification
- Extremely long run times for mixed signal verification (e.g. we looked at typical SAR ADC and we tried to create a typical regression suite for it. This regression suite then took several weeks of pure simulation time)
- Very high verification effort also in setting up the test benches (man-power)

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So far there is no systematic way to verify a analog/mixed signal design

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Trends

- More extensive use of models
- Separate Analog-Mixed-Signal verification engineer (more programming-intensive compared to analog designer)
- In Automotive: ISO26262 demands even more verification tasks (like FMEDA verification, Fault Injection, …)
- Better documentation and traceability of verification
- Automated test benches -> regression testing
- Mixed signal UVM
- Use of requirement database instead of prose specification
- “Verification in the field”: Chip Health Monitoring / Preventive Maintanance
- BISTS to enable „Verification in the field“ over lifetime

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Challenges in AMS-Verificaton

- Model verification
- Convergence topics
- Verification metrics: Fault coverage / test coverage in analog circuits
- Several Power Supply Domains -> Interactions
- With corner simulations there is no guarantee that worst case is covered -> Monte Carlo Simulations take a lot of time
- Automated test benches -> automatic checkers only cover part of the analysis, how to cover the rest?
- No systematic methods available
- No formal methods available

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Challenges in AMS-Verification

- Increasing verification requirements challenge designers and verification engineers
  - Functional verification
  - Parametric verification
  - Post layout verification
  - Corner simulation verification
  - Monte Carlo simulation verification
  - EMC verification
  - ESD verification
  - FMEA/FMEDA verification
  - Verification of „orderly" destruction of chip in case of system failure (especially automotive)
  - „Out of spec" verification (especially automotive)
  - Documentation of verification
  - Reliability/aging verification (reliability over lifetime)
  - Mixed signal UVM leads to exponentially increasing simulations

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Conclusion

- Increasing requirements for AMS-Verification drive verification time and verification effort to uneconomical dimension
- Documentation and traceability efforts explode

New, systematic and efficient ways of AMS-Verification need to be found

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