Artificial Intelligence Solutions for Verification of Analog and Mixed-Signal Smart Power Systems

Ramin M. Hasani[1], **Benjamin Kulnik**[1], **Dieter Haerle**[2], **Radu Grosu**[1]
[1]Cyber-Physical Systems, TU Wien, Austria
[1]KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH, Villach, Austria
Correspondances to: ramin.hasani@tuwien.ac.at

Abstract

In this work, we explore novel artificial intelligence (AI) solutions for the verification of analog and mixed-signal (AMS) complex integrated circuits (IC). The main target is to improve the time performance and the accuracy of the verification process of AMS circuits. In this regard, we develop numerous neural network models for AMS ICs, and utilize such models into the verification process. We show that such methods can result in gaining up to two orders of magnitude speed-up in the fault-injection simulations of ICs. In terms of developmental-efficiency and automation performance, our AI modeling suite is superior over existing methods.

1 Introduction

One challenging issue in the verification process of analog and mixed signal (AMS) ICs is the development of high performance models for carrying out time-efficient simulations. Transistor-level fault simulations of a single IC can take up to one or two weeks to be completed. Figure 1A-left shows the fast-fault-injection method (FFIM) where one can model some parts of the a complex IC with top-level models and inject fault in the transistor-level of the small remaining part of the IC, in order to gain speed-ups in the fault-simulations. Figure 1B demonstrates an accuracy versus performance trade-off between various modeling approaches for the FFIM. In the present study, we propose various neural network (NN) architectures for modeling parts or the entire Analog IC and illustrate their accuracy and time-performance.

2 Methods

NNs are designed in MATLAB and TensorFlow and were integrated into Cadence design environment by the available co-simulation toolboxes such as MATLAB/AMS Designer Cosimulation platform for the MATLAB NN models and Inter-Process Communication for Python models. We now describe various neural network architectures have been designed and to be designed:

2.1 NARX models of ICs

We introduced a black-box method for automatically learning an approximate but simulation-time efficient high-level abstraction of given analog integrated circuit (IC) in [Hasani *et al.*, 2016]. The learned abstraction consists of a nonlinear auto-regressive neural network with exogenous input (NARX), which is trained and validated from the input-output traces of the IC stimulated with particular inputs. We showed the effectiveness of such approach on the power-up behavior and supply dependency of a CMOS band-gap reference circuit (BGR) (See Figure 1D). The approach is scaleable to the modeling of overall behavior of an IC (See Figure 1E as an example of the NARX network architecture).

2.2 Compositional Neural Network Models of ICs

We introduced a compositional method for the construction of a neural-network (NN) capturing the dynamic behavior of a complex analog multiple-input multiple-output (MIMO) system [Hasani *et al.*, 2017]. The method first learns for each input/output pair (i, O), see Figure 1A-right, a small-sized NARX network representing the transfer-function h_{iO}. The training dataset is generated by varying input i of the MIMO, only. Then, for each output O, the transfer functions h_{iO} are combined by a time-delayed neural network (TDNN) layer, f_O. The training dataset for f_O is generated by varying all MIMO inputs. The final output is $f = (f_1, \ldots, f_n)$. The NN's parameters are learned using Levenberg-Marquardt back-propagation algorithm. We applied our method to learn an NN abstraction of a BGR. First, we learned the NARX NNs corresponding to trimming, load-jump and line-jump responses of the circuit. Then, we recomposed the outputs by training the second layer TDNN structure. We demonstrated the performance of our learned NN in the transient simulation of the BGR by reducing the simulation-time by a factor of 17 compared to the transistor-level simulations. Such method allows us to map particular parts of the NN to specific behavioral features of the BGR.

2.3 MLP Models of ICs

Multilayer-perceptrons were employed for modeling of a BGR, and illustrated remarkable accuracy on a test set. Figure 1F shows the output of a BGR together with its 6-layered time-delayed neural nets (TDNN) response. Besides the

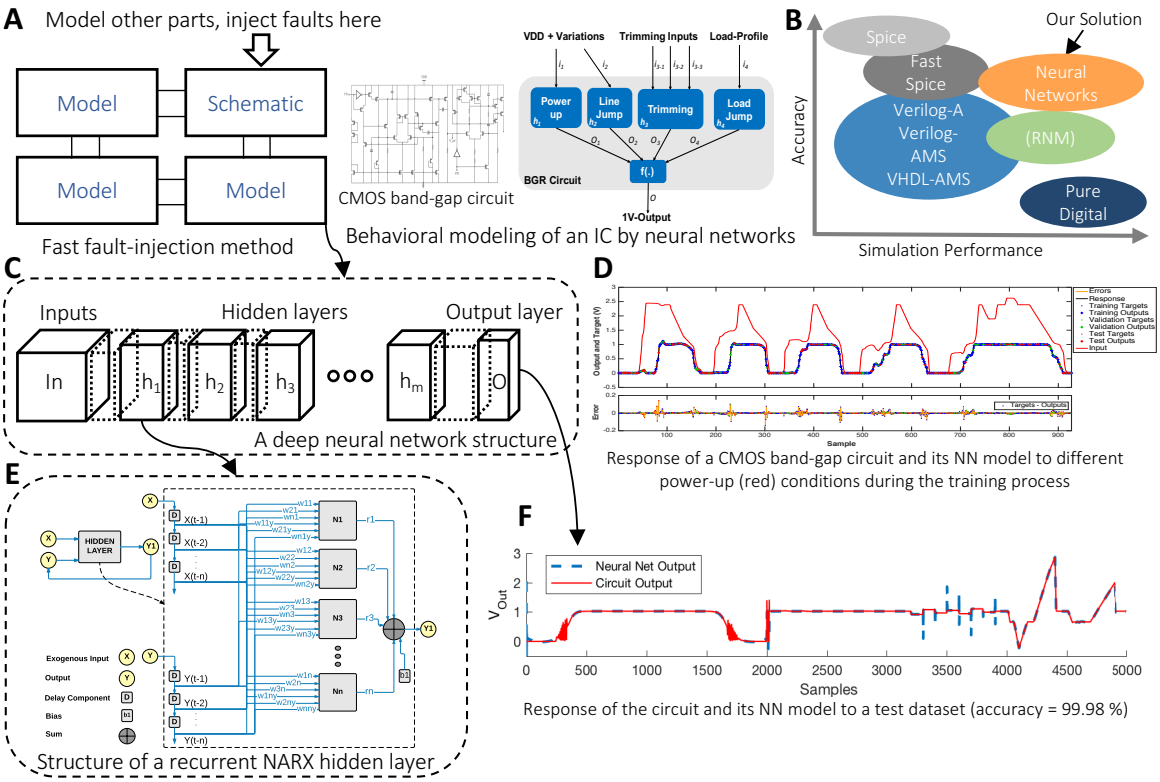

Figure 1: Overview. A) left: fault injection method, middle: a CMOS bad-gap reference circuit (BGR), right: decomposition and recomposition of behavioral functions of a BGR, to be modeled by neural networks. B) A trade-of between accuracy and speed performance of various AMS ICs' modeling approaches. C) Sample architecture of a deep neural net. D) sample learned behavioral feature of a BGR by a NARX network. E) Single layer small-sized NARX network. F) sample output of an IC together with its neural network model after the training process to a test set.

high-level of accuracy, by using such models we gain a simulation speed-up with a factor of 20 up to 50 depending on the circuit while maintaining a high level of accuracy.

2.4 LSTM models of Analog ICs

We are currently developing long short-term memory (LSTM) recurrent networks for modeling CMOS Oscillator, BGR and floating regulator circuits. Our aim is to achieve much better accuracy compared to the previously developed models. Python models are being designed in TensorFlow and will be co-simulated in Cadence environment using Inter-Process Communication (IPC).

3 Next Steps

- Developmet of more integrated circuit's models by neural networks in order to assess the overall pros and cons of the approach
- Trying various architectures of neural networks and benchmark them against each other.
- Find an efficient procedure for inclusion of the NN models into the Cadence design environment.
- Employ our neural network models into the actual verification process of the AMS circuits and evaluate the time-performance and fault-coverage rate of the method.

4 Final Note

Artificial intelligence and in particular deep learning solutions for various industrial applications is rapidly growing towards providing smarter, safer and autonomous methods. Accordingly, within the next couple of years, an improved version of our approach is going to merge existing efficient methods for the verification of AMS ICs into a global autonomous smart verification suit which will presumably turn into the common method for fast and reliable pre-silicon verification of AMS integrated circuits.

References

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