Speeding up Repeated Analog Simulations for Reliability and Testing

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As the use of ICs is becoming ubiquitous, their probability of failure has to be readdressed to cope with the stringent requirements of future cyber-physical systems. Furthermore, deep scaling of technology further agravates the situation by making silicon devices less robust to aging effects. Stringent design and test specifications are necessary to screen out the ICs that would cause failures. To guarantee the reliability and correct functionality of fabricated circuits, many simulations are needed at design time. For developing test programs, fault simulations are needed that require the circuit to be simulated for each defect that can occur, which consists of only a few changes to the circuit for each defect. Another example is the task of automatic test signal generation, where it is not feasible to do an exhaustive search for tests. Can circuit simulators be adapted to include a large number of small changes? Can a circuit simulator find a circuit state under certain voltage or current conditions?

1 Introduction

Cyber-physical systems, such as autonomous vehicles, show an increasing trend in the quantity of employed Integrated Circuits (ICs). This trend causes reliability requirements to become more stringent because of the possibility of defects that may compromise an IC's function. These defects can be divided into two categories: parametric and catastrophic [3]. Furthermore, with IC technologies scaling down further, aging effects become more dominant during IC lifetimes [5]. Technology scaling also enables more complex designs for relatively lower cost, which further deteriorates the situation.

For digital circuits, test escapes are very low, resulting in low failures in the field. Analog ICs, on the other hand, still suffer from relatively high test escapes [2]. This is because analog IC design lacks scalable and automated design and test generation tools. To reduce analog test escapes, design and test simulation tools must be able cope with the future reliability requirements.

2 Simulation Methods and Improvements

Monte Carlo and process corner simulations are used to account for the effects of parametric defects. They model process and random defects that have impact on the device parameters. In the usual case an arbitrary number of these simulations is used for certain process corners to guarantee the functionality of the good ICs in the presence of defects. Their effect is given by a model created by the foundry responsible for fabrication. Process corners are usually fixed to typical, slow and fast, whereas Monte Carlo is random.

Catastrophic defects, while being random in occurrence, can be exhaustively simulated. An example of a fault model for catastrophic defects in transistors is the 6-fault model [4]. Such models cause the

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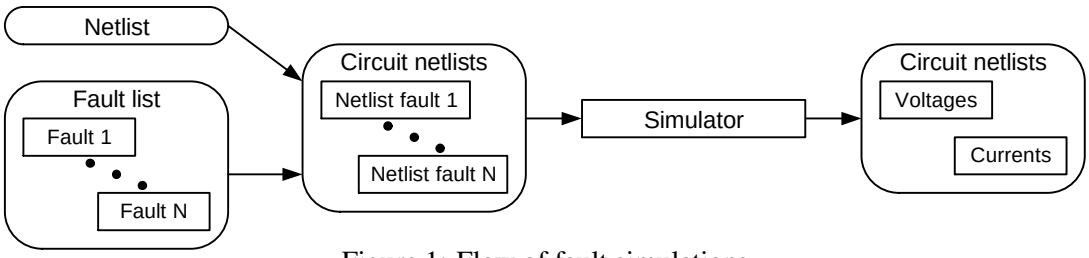

Figure 1: Flow of fault simulations.

number of required simulations to scale with the amount of transistors, on top of the time complexity of the circuit analysis algorithms.

The simulation flow is given in Figure 1. A circuit is described by its netlist, then a fault list is used to generate as many netlists as there are faults. Then a simulator such as Hspice or Spectre is used to simulate each netlist. This results in a characterization of the circuit for each defect.

One solution for speedup is to first partition the circuit into smaller blocks, then generate a look-up table for node currents in function of node voltages [1]. A look-up table is also generated for each defect. Look-up table access replaces solving a set of non-linear equations, hence speeding up the process. However, any function approximation can be used as well. As long as the approximation function is invertible, it is possible to use this method to generate a certain voltage in an internal node as well as propagate signal to measureable nodes such that defects can be detected. Another solution is to integrate faults inside the simulation algorithms, such that many faults are simulated at once. For DC analysis, for example, this would mean including defects in the non-linear equation solver. The efficiency of these and other approaches will needed to be evaluated on practical circuits of industrial size.

3 Conclusions

A speedup of fault simulations for analog circuits is necessary to ensure the future reliability requirements. Possible solutions to this problem include rebuilding the simulations algorithms to accomodate faults and using the current simulators to build faster structures and continue using it. A horough analysis of different methods is needed in order to obtain a practical approach towards enabling better analog IC tests.

References

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